NEC

MOS INTEGRATED CIRCUIT

μPD77C25, 77P25

DIGITAL SIGNAL PROCESSOR

The μPD77C25, 77P25 are 16-bit fixed point CMOS signal processors intended for real-time digital processing of speech signals.

Each device consists of a parallel multiplier (16 x 16 bits → 31 bits), an ALU (16 bits), an instruction ROM (2,048 x 24 bits), a data ROM (1,024 x 16 bits), a data RAM (256 x 16 bits), I/O ports, and others. All instructions consist of 24 bits or one word instruction are executed in 122 ns (at f_{CLK} = 8.192 MHz) including sum of product computations.

Since signals that interfaces with the host CPU are provided, the μPD77C25, 77P25 can cover a variety of applications, serving as an I/O processor. Moreover, they can also be used as single-chip CPU.

The μPD77C25, 77P25 provide an instruction ROM each four times larger than that of the former product μPD7720 signal processor. Additionally, each device has a data ROM and a data RAM, both of which are two times larger, and a processing speed faster. Furthermore, the μPD77C25, 77P25 can replace the μPD7720 as they have the same pin connections.

The instruction sets of the μPD77C25, 77P25 are upward-compatible with that of the μPD7720 at the assembler source program level.

The μPD77C25 is version with on-chip resources including the instruction ROM and data ROM are constructed in mask ROMs; the μPD77P25 has PROMs. The μPD77P25D is an UVEPROM type and the μPD77P25C/L/GW is an one time PROM (OTP) type.

Remark In this document, the μPD77C25 refers to the μPD77C25, 77P25 unless otherwise specified.

FEATURES

- Biquad Digital Filter (with sampling performed at 8 kHz) : Equivalent to 113 filters
- On-chip exclusive parallel multiplier : 16 bits x 16 bits → 31 bits
- Instruction ROM : 2,048 words x 24 bits
- Data ROM : 1,024 words x 16 bits
- Data RAM : 256 words x 16 bits
- Dual accumulator method
- On-chip serial input and serial output interfaces
- On-chip host CPU bus interface
- On-chip DMA interface
- Upward-compatible with the μPD7720 at assembler source program level
- Pin-compatible with μPD7720
- Low-power CMOS

The information in this document is subject to change without notice.

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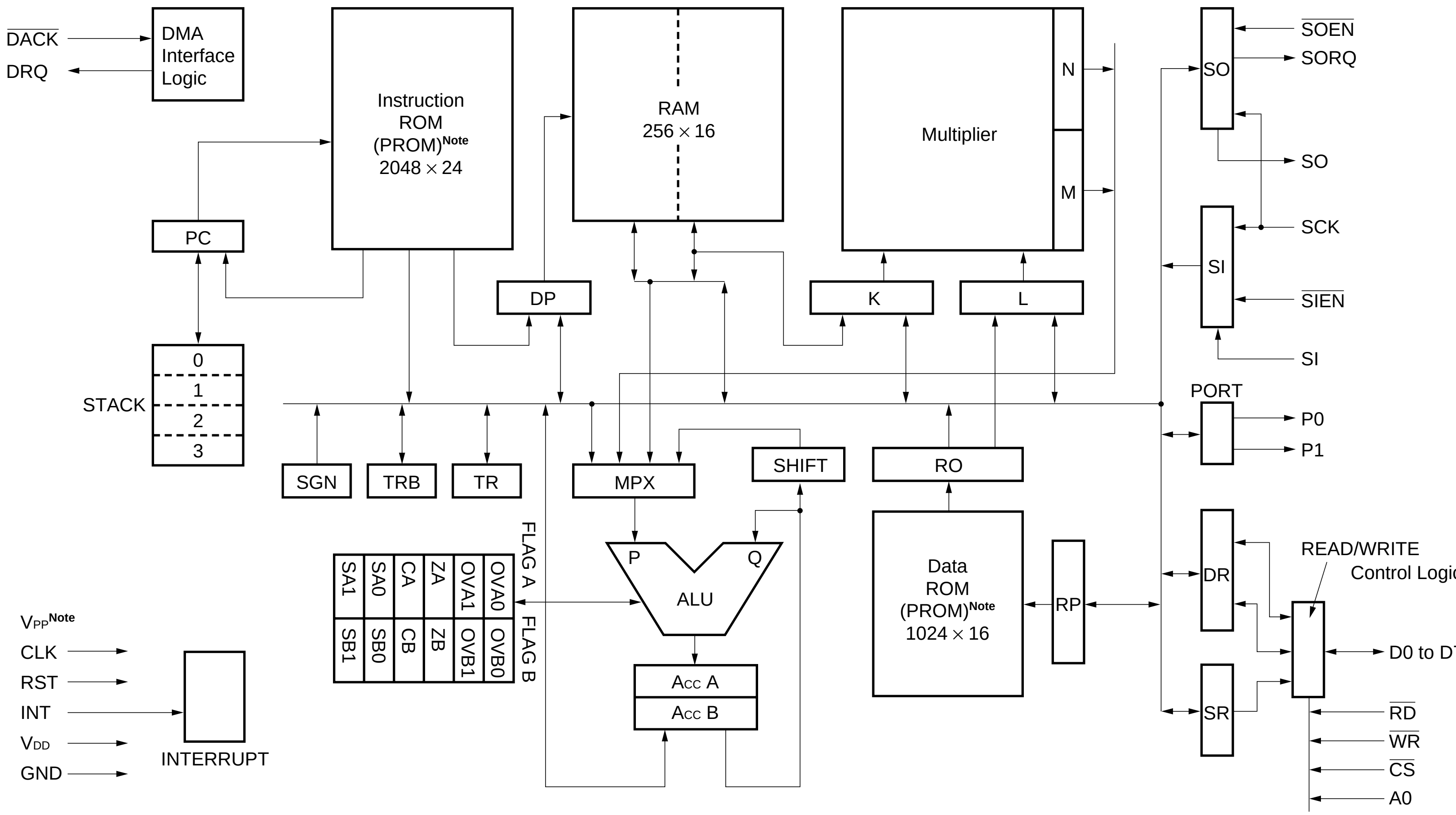
The mark ★ shows major revised points.

★ ORDERING INFORMATION

Part Number	Package
μPD77C25C-xxx	28-pin plastic DIP (600 mil)
μPD77C25GW-xxx	32-pin plastic SOP (525 mil)
μPD77C25L-xxx	44-pin plastic QFJ (650 x 650 mil)
μPD77P25C	28-pin plastic DIP (600 mil)
μPD77P25D	28-pin ceramic DIP (600 mil)
μPD77P25GW	32-pin plastic SOP (525 mil)
μPD77P25L	44-pin plastic QFJ (650 x 650 mil)

Remark xxx is a ROM code suffix.

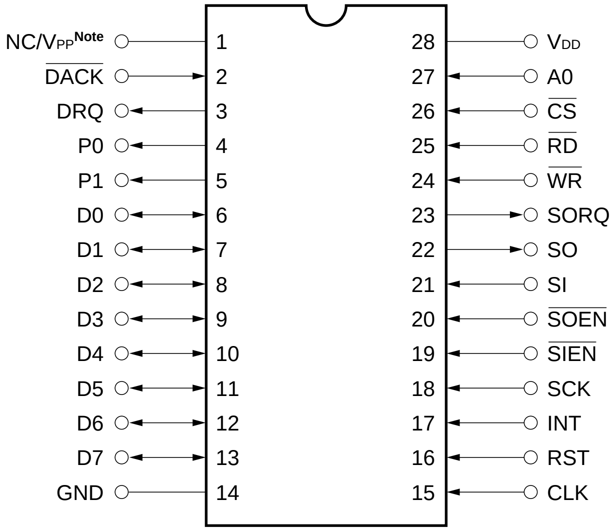
BLOCK DIAGRAM



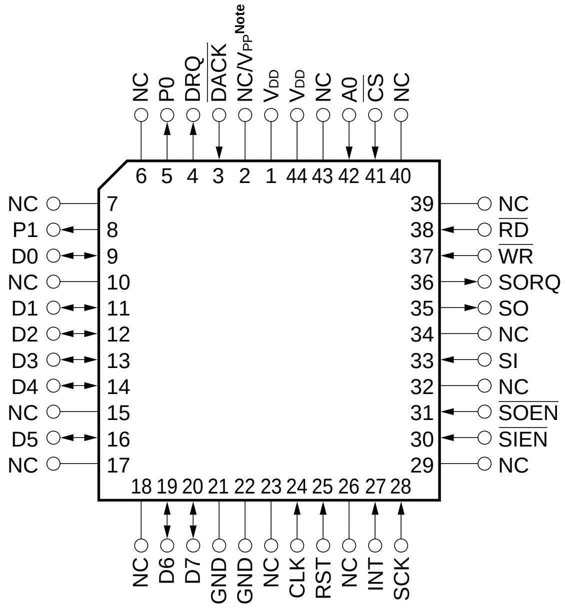
Note μPD77P25

★ PIN CONFIGURATIONS (Top View)

28-pin plastic DIP (600 mil): μPD77C25C-xxx, μPD77P25C
28-pin ceramic DIP (600 mil): μPD77P25D

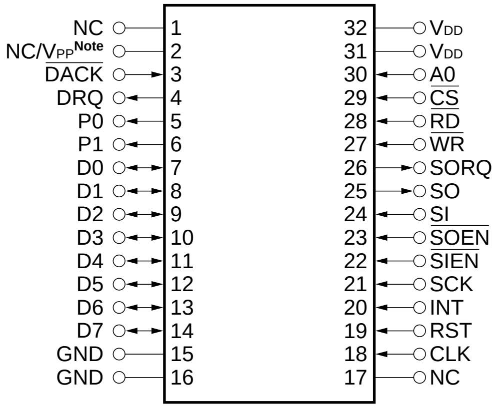


44-pin plastic QFJ (650 x 650 mil): μPD77C25L-xxx, μPD77P25L



Note NC for μPD77C25
V_{PP} for μPD77P25

32-pin plastic SOP (525 mil): μPD77C25GW-xxx, μPD77P25GW



Note NC for μPD77C25
V_{PP} for μPD77P25

A0	:	Address Input	RST	:	Reset Input
CLK	:	Clock Input	SCK	:	Serial Data Clock
$\overline{CS}$	:	Chip Select Input	SI	:	Serial Data Input
$\overline{DACK}$	:	DMA Acknowledge Signal Input	$\overline{SIEN}$	:	Serial Input Enable
DRQ	:	DMA Request Signal Output	SO	:	Serial Data Output
D0 to D7	:	Data Bus Input/Output	$\overline{SOEN}$	:	Serial Output Enable
GND	:	Ground	SORQ	:	Serial Output Request Signal Output
INT	:	Interrupt Input	V_{DD}	:	Power Supply
NC	:	No Connection	V_{PP}	:	Power Supply
P0, P1	:	General Purpose Output Port	$\overline{WR}$	:	Write Signal Input
$\overline{RD}$	:	Read Signal Input			

DIFFERENCES BETWEEN μPD77C25 AND μPD7720 FAMILY

The μPD77C25 has enhanced functions of the conventional μPD7720 16-bit signal processor family and thus is compatible with the μPD7720 family at an assembler source program level.

Differences between μPD77C25 and μPD7720 family is shown below.

Differences between μPD77C25 and μPD7720 Family

Item		μPD7720	μPD77C25
Memory	Instruction ROM	512 x 23 bits	2,048 x 24 bits
	Data ROM	510 x13 bits	1,024 x 16 bits
	RAM	128 x 16 bits	256 x 16 bits
Register	PC	9 bits	11 bits
	STACK	9 bits x 4 levels	11 bits x 4 levels
	RP	9 bits	10 bits
	RO	13 bits	16 bits
	DP	7 bits	8 bits
	TRB	without	with
Instruction length		23 bits (w/3-bit DP_H.M field)	24 bits (w/4-bit DP_H.M field)
Added instructions		—	JDPLNO JDPLNF M8 to MF (Modified DP)
RQM flag operations		Not affected in DMA mode	Affected even in DMA mode
Operation clock (Instruction cycle)		8.192 MHz (244 ns)	77C25: 8.192 MHz (122 ns)
Serial interface clock		2.048 MHz	77C25: 4.096 MHz

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Functions for Normal Operation

Pin Designation	Pin Number			I/O	Function
	28-pin Plastic DIP, 28-pin Ceramic DIP	32-pin Plastic SOP	44-pin Plastic QFJ		
V_{DD}	28	31 32	1 44	—	Power input pin. Inputs +5 V.
GND	14	15 16	21 22	— —	Ground pin
V_{PP} Note	1	2	2	—	Program power input pin of internal PROM. Connected to +12.5 V for programming PROM or to +5 V for normal operation.
CLK	15	18	24	I	Inputs system clock having frequency as high as instruction cycle.
RST	16	19	25	I	Inputs system reset signal (active high). Width of signal must be wider than 2 system clock periods.
INT	17	20	27	I	Inputs mask able interrupt signal (active high). Program execution jumps to interrupt address at rising edge of this pin and with interrupt enabled.
$\overline{CS}$	26	29	41	I	Inputs chip select signal (active low). "0" input to this pin enables read/write operation by host CPU via D0 through D7.
A0	27	30	42	I	Inputs address signal. Signal input to this pin selects register whose contents are to be output from D0 through D7 during read operation. "0" selects DR and "1", SR.
$\overline{RD}$	25	28	38	I	Inputs read signal (active low). "0" to this pin causes D0 through D7 to output data (with $\overline{CS}$ = "0").
$\overline{WR}$	24	27	37	I	Inputs write signal (active low). "0" to this pin causes D0 through D7 to input data (with $\overline{CS}$ = "0").
D0 to D7	Refer to PIN CONFIGURATION	Refer to PIN CONFIGURATION	Refer to PIN CONFIGURATION	I/O (3-state)	Constitute 8-bit data bus for host CPU and perform input/output according to $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$.
DRQ	3	4	4	O	Outputs DMA request signal (active high) and requests data transfer in DMA mode.

★ **Note** This pin serves as V_{PP} only for the μPD77P25 and is NC for the μPD77C25.
When designing the μPD77C25 application system compatible with the μPD77P25, it is no problem to supply +5 V to pin 1.

Pin Designation	Pin Number			I/O	Function
	28-pin Plastic DIP, 28-pin Ceramic DIP	32-pin Plastic SOP	44-pin Plastic QFJ		
$\overline{\text{DACK}}$	2	3	3	I	Inputs DMA acknowledge signal (active low). "0" is input when DMA is enabled. When $\overline{\text{DACK}}$ = "0", this pin performs similar operation to when CS = "0" and A0 = "0". Since it is always valid, input "1" when DMA is not used.
P0, P1	4 5	5 6	5 8	O	Constitute general-purpose output port.
SI	21	24	33	I	Inputs serial data which is read into the processor in synchronization with rising edge of SCK clock.
$\overline{\text{SIEN}}$	19	22	30	I	Inputs serial input enable signal (active low) to enable serial data input from SI. This signal must be kept high level during the RST is high level and two instruction cycles after the RST becames low level.
SO	22	25	35	O (3-state)	Outputs serial data which is output in synchronization with falling edge of SCK clock.
$\overline{\text{SOEN}}$	20	23	31	I	Outputs serial output enable signal (active low) to enable serial data output from SO. This signal must be kept high level during the RST is high level and two instruction cycles after the RST becames low level.
SORQ	23	26	36	O	Outputs serial output request signal (active high). It is set to "1" when output data are set in SO register and cleared to "0" when on completion of output.
SCK	18	21	28	I	Inputs serial data clock with which serial data input/output is synchronized.

1.2 Pin Functions for Programming/reading μPD77P25's Internal PROM

Pin Name	Pin Number			Pin Name for Normal Operation	Function
	28-pin Plastic DIP, 28-pin Ceramic DIP	32-pin Plastic SOP	44-pin Plastic QFJ		
A0	27	30	42	A0	Input address (viewed from external device) for programming/reading PROM (instruction ROM and data ROM).
A1	24	27	37	$\overline{WR}$	
A2	23	26	36	SORQ	
A3	22	25	35	SO	
A4	21	24	33	SI	
A5	20	23	31	$\overline{SOEN}$	
A6	19	22	30	$\overline{SIEN}$	
A7	18	21	28	SCK	
A8	17	20	27	INT	
A9	15	18	24	CLK	
A10	5	5	8	P1	
A11	4	6	5	P0	
A12	3	4	4	DRQ	
A13	2	3	3	$\overline{DACK}$	
D0 to D7	6 to 13	7 to 14	9 11 to 14 16 19, 20	D0 to D7	Inputs/outputs data for PROM (instruction ROM and data ROM)
$\overline{CE}$	26	29	41	$\overline{CS}$	PROM program strobe signal (active low)
$\overline{OE}$	25	28	38	$\overline{RD}$	PROM read strobe signal (active low)
V_{PP}	1	2	2	V_{PP}	Power pin for programming PROM Apply +12.5 V for writing and +5 V for reading.
V_{DD}	28	32 31	1 44	V_{DD}	Power pin Apply +6 V for programming and +5 V for reading.
GND	14	15 16	21 22	GND	Ground pin
—	16	19	25	RST	Sets PROM program or read mode. Mode is set when +12.5 V is applied.

2. INTERNAL FUNCTIONS

(1) Instruction ROM

This ROM stores the program of the μPD77C25 and has a capacity of 2K words x 24 bits. In the μPD77C25 this is a mask ROM and in the μPD77P25 is a PROM. The address to be accessed is specified by Program Counter (PC).

(2) PC (Program Counter)

This is a 11-bit binary counter which specifies an address of the instruction ROM. Usually, the contents of PC are incremented by one each time an instruction is fetched, and accordingly the instructions are read from ROM in order.

When jump instruction or subroutine call instruction is executed, the NA (Next address) field value of the instruction is input to the PC. The return address saved in the stack is input to the PC in case that the return instruction is executed, and the interrupt address (100H) is input in case that an interrupt request is input to the INT pin with the interrupt enabled.

The reset input clears the PC contents to 00H and the program execution starts from address 0.

(3) STACK

The stack has 11 bit x 4 level, LIFO (Last-In First-Out) configuration and stores the return address when the subroutine call instruction is executed or an interrupt is generated. The return address is read out from the stack and input to the PC when the return instruction is executed.

(4) RAM

The RAM stores the data and is configured of 256 words x 16 bits. The address to be accessed is specified by Data Pointer (DP). In addition to transferring data to and from the internal data bus, the RAM can directly output data to the P input of ALU. It can also directly output to the K register the address data with DP6 replaced with “1”.

(5) DP (Data Pointer)

The data pointer is an 8-bit register which specifies a RAM address. It is connected to the lower 8 bits of the internal data bus, and transfers data to and from the other registers through it.

The upper 4 bits of DP (DPH) can be qualified when exclusively ORed with the 4 bits of the DPHM field in an instruction.

The contents of the lower 4 bits of DP (DPL) can be incremented, decremented, or cleared depending on the specification of the DPL field in an instruction.

(6) Data ROM

The data ROM is a mask ROM in the μPD77C25 and a PROM in the μPD77P25. It stores various fixed data such as coefficients of filter and has a capacity of 1K words x 16 bits. The address to be accessed is specified by ROM Pointer (RP) and is output to the data bus and the input register L of the multiplier through ROM Output Buffer (RO).

(7) RP (ROM Pointer)

The ROM Pointer is a 10-bit register which specifies a data ROM address to be accessed. It is connected to the lower 10 bits of the internal data bus.

The contents of RP can be decremented by specifying the RPDCR bit of an instruction.

(8) RO (ROM Output Buffer)

The ROM output buffer is a 16 bits register which holds the data output by the data ROM. The contents of this register are directly output to the internal data bus and the input register L of the multiplier.

(9) Multiplier

This is a parallel multiplier using secondary Booth's algorithm. It multiplies the 2's complement of the 16-bit data stored in the K and L registers in each instruction cycle. As a result, a sign bit and 30-bit data are obtained. The multiplier then stores the sign bit and the upper 15 bits of the 30-bit data in the M register. The lower 15 bits are stored in the upper 15 bits of the N register. ("0" is stored in the LSB.)

(10) K and L registers

These are 16-bit registers which hold the data input from the multiplier. The K register can not only directly input the data from RAM but also transfer data to and from the internal data bus. The L register can directly input the data from the data ROM, in addition, it can transfer data to and from the internal data bus. The data which are input to the K and L registers are input to the multiplier simultaneously, and performs an arithmetic operation.

(11) M and N registers

These are 16-bit registers which hold the results of the multiplication performed by the multiplier. The upper 16 bits of the multiplication results (i.e., sign bit plus the upper 15 bits) are stored in the M register. The lower 15 bits are stored in the N register ("0" is stored in the LSB). Both the M and N registers are connected to the P input of the ALU.

(12) ALU and AccA, AccB

The ALU performs the following arithmetic operations of 16-bit data on two inputs: P and Q.

- OR
- AND
- XOR (Exclusive OR)
- SUB
- ADD
- Shift (only AccA and AccB)
- 1's complement (only AccA and AccB)

P input: RAM, Internal DATA bus, M register, N register, SHIFT, 0000 (H)

Q input: AccA, AccB

Both AccA and AccB are 16-bit accumulators which store the results of the arithmetic operation performed by the ALU. They are connected to the output of the ALU and the internal data bus. The ASL field of an instruction specifies which accumulator is to be used. The contents of AccA and AccB can be output to the internal data bus, and can input to Q input of the ALU and SHIFT.

(13) SHIFT

This is a register which shifts 16-bit data input from AccA and AccB. 1-bit shift right, 1-bit shift left, 2-bit shift left, 4-bit shift left, and 8-bit exchange can be performed.

(14) Flag registers FLAG A and FLAG B

FLAG A and FLAG B are both 6-bit registers that hold the result of the ALU operation. FLAG A operates when AccA is selected, while FLAG B operates when AccB is selected.

FLAG A and FLAG B consist of the following flag bits:

FLAG A	SA1	SA0	CA	ZA	OVA1	OVA0
FLAG B	SB1	SB0	CB	ZB	OVB1	OVB0

(a) CA, CB (Carry)

The flags store the carry or borrow resulting from the executed operation. (OPERATION: SUB, ADD, SBB, ADC, DEC, INC)

(b) ZA, ZB (Zero)

The flags are set to “1” if the result of the executed operation is “0”; otherwise, cleared to “0”.

(c) SA0, SB0 (Sign 0)

The flags store the sign bit (MSB) of the result of the operation.

(d) OVA0, OVB0 (Overflow 0)

The flags are set to “1” if an overflow in positive or negative direction has occurred as a result of the executed operation; otherwise, cleared to “0”.

(e) OVA1, OVB1 (Overflow 1)

The flags set to “1” if an overflow has occurred the odd number of times as a result of the 3 operations executed, and set to “0” if it has occurred the even number of times. (OPERATION: SUB, ADD, SBB, ADC, DEC, INC)

(f) SA1, SB1 (Sign 1)

The flags are used with OVA1 or OVB1 to effectively process overflow. These indicates the direction in which the overflow (positive or negative) has, if any, occurred.

(15) TR, TRB (Temporary Register)

TR and TRB are 16-bit general-purpose registers which can be used to temporary latch data. They are connected to the internal data bus.

(16) SGN (Sign Register)

SGN is set to 8000H if the SA1 flag is “0” and to 7FFFH if the flag is “1”. Therefore, the overflow compensation can be performed with one instruction by simply transferring the contents of the SGN register without a test instruction.

(17) SR (Status Register)

The status register is a register which hold the status the μPD77C25 needs to transfer data to/from external devices. It is internally handled as a 16-bit register, and the upper 8 bits can be read from an external device through D0 to D7 pins.

MSB							8	
RQM	USF1	USF0	DRS	DMA	DEC	SOC	SIC	Can be read out from D0 to D7 pins.

7							LSB
EI	0	0	0	0	0	P1	P0

(a) P0, P1

The P0 and P1 correspond to output ports P0 and P1, and to which values input to these bits are directly output.

(b) EI (Enable Interrupt)

EI is the bit to specify whether enables or disables interrupt.

"0": Interrupt is disabled.

"1": Interrupt is enabled.

(c) SIC (SI Control)

SIC is the bit to specify the length of serial data input to SI pins.

"0": The length of serial input data is specified 16-bit.

"1": The length of serial input data is specified 8-bit.

(d) SOC (SO Control)

SOC is the bit to specify the length of serial data output to SO pins.

"0": The length of serial output data is specified 16-bit.

"1": The length of serial output data is specified 8-bit.

(e) DRC (DR Control)

DRC is the bit to specify the length of data transfer to and from host CPU.

"0": 16-bit length is specified.

"1": 8-bit length is specified.

(f) DMA (Direct Memory Access)

DMA is the bit to specify mode to transfer data to and from host CPU.

"0": non-DMA mode is specified.

"1": DMA mode is specified.

(g) DRS (DR Status)

DRS is the bit to indicate data transfer status of DR register in case of transferring 16-bit data. (DRC = 0)

"0": It indicates transfer is terminated. (8-bit data is transferred two times.)

"1": It indicates transfer is in progress.

(h) USF0, USF1 (User's Flag)

USF0 and USF1 are the flag bits which can be freely used by user and can be used as a status bit in transferring data to/from external device.

(i) RQM (Request for Master)

RQM is the bit to indicate that μPD77C25 is requesting host CPU for data write/read.

"0": It indicates that data read/write is externally performed.

"1": It indicates that DR register is internally read/written.

This flag bit also changes in DMA mode.

(18) PORT

Ports are internally assigned to the same address as SR register (P0, P1) and can be used as output ports to external devices.

(19) DR (Data Register)

DR is the 16-bit register to interface to/from CPU. Since it is externally connected to the 8-bit bus, data is read from/written to external in units of 8 bits. Internally writing and reading are performed by 16-bit at a time. When the 8-bit mode is specified by DRC bit, only the lower 8 bits of the DR register (16 bits long) are valid.

(20) READ/WRITE Control Logic

R/W logic constructs the control part to transfer data to/from external devices through D0-D7. The following operations are performed depending on the status of $\overline{CS}$, A0, $\overline{RD}$, and $\overline{WR}$.

$\overline{CS}$	A0	$\overline{WR}$	$\overline{RD}$	Function
1	X	X	X	Internal operation is not affected.
X	X	1	1	D0-D7 are at high impedance levels.
0	0	0	1	Data on D0 to D7 are latched to DR register.[Note]
0	0	1	0	Contents of DR are output D0-D7.[Note]
0	1	0	1	Inhibit (SR is read only)
0	1	1	0	Eight MSBs of SR are output to D0-D7.
0	X	0	0	Inhibit (may not read and write simultaneously)

Note Eight MSBs or 8 LSBs of data register (DR) are used, depending on DR status bit (DRS).

(21) DMA Interface Logic

DMA Interface Logic controls DRQ signal using $\overline{DACK}$ signal. DRQ signal requests data transfer between DR register and external host processor or memory.

(22) SI (Serial Input Register)

The serial data from an external devices is input to the SI register. The data are taken into the register in synchronization of SCK, and are changed to the parallel data by the register. The parallel data is output to the internal data bus by the instruction. The serial data can be treated not only LSB first but MSB first.

(23) SO (Serial Output Register)

This register loads the parallel data to be output from the internal data bus, and changes the data into serial, then outputs to the external devices. It can treat both LSB-first data and MSB-first data. The serial data is output in synchronization of SCK.

(24) INTERRUPT

This is the part to execute the interrupt process. An interrupt is detected at the rising edge of the INT signal when the EI bit of the SR register is set to “1”. When the interrupt is accepted, the interrupt process that address is from 100H is executed.

(25) RST (Reset)

The followings are initialized to “0” by the RST signal.

- PC
- FLAG A, FLAG B
- SR register
- DRQ
- SORQ
- SI ACK flag, SO ACK flag

RP register is set to “3FFH”. The other registers and contents of DATA RAM are not changed.

3. INSTRUCTION

All instructions of the μPD77C25 are one word instruction; one instruction is composed of 24 bits. The instructions are divided into the following four types.

OP instruction : This instruction is used to perform operations such as ordinary arithmetic operations and data transfer.

RT instruction : This instruction is return instruction.

JP instruction : This instruction causes unconditional or conditional jump of program execution, or calls a subroutine.

LD instruction : This loads 16-bit immediate data to the specified register.

3.1 OP Instruction

<table>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">00</td><td colspan="2">P-SELECT</td><td colspan="4">ALU</td><td>ASL</td><td colspan="2">DP_L</td><td colspan="4">$DP_H \cdot M$</td><td>RPDCR</td><td colspan="4">SRC</td><td colspan="4">DST</td></tr>
</table>

OP instruction has the following functions.

(i) This instruction consists of six fields and two bits.

(ii) Program Counter is incremented to the address hold at that time.

(1) P-SELECT Field

This field selects P input of ALU.

(2) ALU Field

This field specifies ALU operation.

(3) ASL (Acc Selection) bit

This bit selects Q input of ALU and specifies AccA or AccB.

(4) DP_L Field

This field specifies operation of lower 4 bits of DP (Data Pointer). The new value of DP_L specified by this field becomes valid from the next instruction.

(5) DP_H•M (DP_H Modify) Field

This field qualifies changes value of the upper 4 bits of DP (Data Pointer). The value of this field is qualified exclusively ORed with the value of the upper 4 bits in DP (Data Pointer). The qualified value of DP_H valid from the next instruction.

(6) RPDCR (RP Decrement) bit

This bit specifies decrement operation of RP (ROM Pointer). The decremented value becomes valid from the next instruction.

(7) SRC (Source) Field

This field specifies source register to the internal data bus for transfer instruction.

(8) DST (Destination) Field

This field specifies the destination register for a transfer instruction. The data specified in SRC Field (output to the internal data bus) is written to the specified register.

3.2 RT Instruction

23–22	21–20	19–16	15	14–13	12–9	8	7–4	3–0
01	P-SELECT	ALU	ASL	DP_L	$DP_H \cdot M$	RPDCR	SRC	DST

RT instruction is a return instruction and has the following functions.

(1) This instruction consists of six fields and two bits like the OP instruction.

(2) It restores the return address saved to the stack to PC after performing the same operation as the OP instruction.

3.3 JP Instruction

23–22	21–13	12–2	1–0
10	BRCH	NA	

JP instruction causes program execution of jump unconditionally or conditionally. It also calls a subroutine.

(1) BRCH (Branch) Field

This field specifies type of jump instruction and conditional jump instruction.

(2) NA (Next Address) Field

This field specifies jump address.

3.4 LD Instruction

23–22	21–6	5–4	3–0
11	ID		DST

This is an immediate data load instruction which loads 16-bit data to the specified register.

(1) ID (Immediate Data) Field

This field specifies the immediate 16-bit data. The immediate data is loaded to the register specified in DST field.

(2) DST (Destination) Field

This field specifies the register that the data specified by ID field is loaded to. This field is the same as DST field in OP instruction.

3.5 Instruction Code

THE LIST OF INSTRUCTION CODE

<table>
<tr><th>Bit / Instruction</th><th>D 23</th><th>D 22</th><th>D 21</th><th>D 20</th><th>D 19</th><th>D 18</th><th>D 17</th><th>D 16</th><th>D 15</th><th>D 14</th><th>D 13</th><th>D 12</th><th>D 11</th><th>D 10</th><th>D 9</th><th>D 8</th><th>D 7</th><th>D 6</th><th>D 5</th><th>D 4</th><th>D 3</th><th>D 2</th><th>D 1</th><th>D 0</th></tr>
<tr><td>OP</td><td colspan="2">0 0</td><td colspan="2">P-SELECT</td><td colspan="4">ALU</td><td>ASL</td><td colspan="2">DP_L</td><td colspan="4">DP_H•M</td><td>RPDCR</td><td colspan="4">SRC</td><td colspan="4">DST</td></tr>
<tr><td>RT</td><td colspan="2">0 1</td><td colspan="22">Same as OP instruction</td></tr>
<tr><td>JP</td><td colspan="2">1 0</td><td colspan="9">BRCH</td><td colspan="11">NA</td><td colspan="2"></td></tr>
<tr><td>LD</td><td colspan="2">1 1</td><td colspan="16">ID</td><td colspan="2"></td><td colspan="4">DST</td></tr>
</table>

ALL INSTRUCTIONS

Instruction	OP field		Contents of instruction
	D_{23}	D_{22}	
OP	0	0	Arithmetic and Transfer Operation
RT	0	1	Return Instruction
JP	1	0	Jump Instruction
LD	1	1	Immediate Data Load Instruction

OP, RT INSTRUCTIONS

Mnemonic	P-SELECT field		Input Data
	D_{21}	D_{20}	
RAM	0	0	RAM
IDB	0	1	Internal Data Bus
M	1	0	M register
N	1	1	N register

OP, RT INSTRUCTIONS

Mnemonic	ALU field				Function	
	D_{19}	D_{18}	D_{17}	D_{16}		
NOP	0	0	0	0	No Operation	
OR	0	0	0	1	OR	(Acc) ← (Acc) v (P)
AND	0	0	1	0	AND	(Acc) ← (Acc) ^ (P)
XOR	0	0	1	1	Exclusive OR	(Acc) ← (Acc) ∀ (P)
SUB	0	1	0	0	Subtract	(Acc) ← (Acc) – (P)
ADD	0	1	0	1	Add	(Acc) ← (Acc) + (P)
SBB	0	1	1	0	Subtract with Borrow	(Acc) ← (Acc) – (P) – (C)
ADC	0	1	1	1	Add with Carry	(Acc) ← (Acc) + (P) + (C)
DEC	1	0	0	0	Decrement Acc	(Acc) ← (Acc) – 1
INC	1	0	0	1	Increment Acc	(Acc) ← (Acc) + 1
CMP	1	0	1	0	Complement Acc (1's complement)	(Acc) ← ($\overline{Acc}$)
SHR1	1	0	1	1	1-bit R-Shift	
SHL1	1	1	0	0	1-bit L-Shift	
SHL2	1	1	0	1	2-bit L-Shift	
SHL4	1	1	1	0	4-bit L-Shift	
XCHG	1	1	1	1	8-bit Exchange	

OP, RT INSTRUCTIONS

Mnemonic	ASL bit	Selection for Acc and FLAG
	D_{15}	
ACCA	0	Acc A
ACCB	1	Acc B

OP, RT INSTRUCTIONS

Mnemonic	DP_L field		Operation
	D_{14}	D_{13}	
DPNOP	0	0	No Operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

OP, RT INSTRUCTIONS

Mnemonic	DP_H•M field				Exclusive OR
	D_{12}	D_{11}	D_{10}	D_9	
M0	0	0	0	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 0\ 0\ 0)$
M1	0	0	0	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 0\ 0\ 1)$
M2	0	0	1	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 0\ 1\ 0)$
M3	0	0	1	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 0\ 1\ 1)$
M4	0	1	0	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 1\ 0\ 0)$
M5	0	1	0	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 1\ 0\ 1)$
M6	0	1	1	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 1\ 1\ 0)$
M7	0	1	1	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (0\ 1\ 1\ 1)$
M8	1	0	0	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 0\ 0\ 0)$
M9	1	0	0	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 0\ 0\ 1)$
MA	1	0	1	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 0\ 1\ 0)$
MB	1	0	1	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 0\ 1\ 1)$
MC	1	1	0	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 1\ 0\ 0)$
MD	1	1	0	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 1\ 0\ 1)$
ME	1	1	1	0	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 1\ 1\ 0)$
MF	1	1	1	1	$(DP_7\ DP_6\ DP_5\ DP_4) \forall (1\ 1\ 1\ 1)$

OP, RT INSTRUCTIONS

Mnemonic	RPDCR bit	Operation
	D_8	
RPNOP	0	No Operation
RPDEC	1	Decrement RP

OP, RT INSTRUCTIONS

Mnemonic	SRC field				Specified register
	D_7	D_6	D_5	D_4	
NON[Note 1], TRB	0	0	0	0	TRB register
A	0	0	0	1	Acc A register
B	0	0	1	0	Acc B register
TR	0	0	1	1	TR register
DP	0	1	0	0	DP register
RP	0	1	0	1	RP register
RO	0	1	1	0	RO register
SGN	0	1	1	1	SGN register
DR	1	0	0	0	DR register
DRNF	1	0	0	1	DR register[Note 2]
SR	1	0	1	0	SR register
SIM	1	0	1	1	SI register (1st → MSB)[Note 3]
SIL	1	1	0	0	SI register (1st → LSB)[Note 4]
K	1	1	0	1	K register
L	1	1	1	0	L register
MEM	1	1	1	1	RAM

Notes
1. The contents of the TRB register are also output if NON is specified.
2. Although the contents of the DR register are output to the internal data bus, the RQM flag is not set. Neither is the DRQ flag in DMA mode.
3. With the 16-bit data, the serial data input first is output to the MSB of the internal data bus; the data input last is output to the LSB.
4. With the 16-bit data, the serial data input first is output to the LSB of the internal data bus; the data input last is output to the MSB.

OP, RT, LD INSTRUCTIONS

Mnemonic	DST field				Specified register
	D_3	D_2	D_1	D_0	
@NON	0	0	0	0	No specified register
@A	0	0	0	1	Acc A register
@B	0	0	1	0	Acc B register
@TR	0	0	1	1	TR register
@DP	0	1	0	0	DP register
@RP	0	1	0	1	RP register
@DR	0	1	1	0	DR register
@SR	0	1	1	1	SR register
@SOL	1	0	0	0	SO register (LSB → 1st)[Note 1]
@SOM	1	0	0	1	SO register (MSB → 1st)[Note 2]
@K	1	0	1	0	K register
@KLR	1	0	1	1	KLR[Note 3]
@KLM	1	1	0	0	KLM[Note 4]
@L	1	1	0	1	L register
@TRB	1	1	1	0	TRB register
@MEM	1	1	1	1	RAM

Notes **1.** With 16-bit data, the serial output is sequentially performed from the LSB bit of the internal data bus.

2. With 16-bit data, the serial output is sequentially performed from the MSB of the internal data bus.

3. The data on the internal bus and the output from the RO register (ROM) are set to the K and L registers, respectively.

4. The data on the internal bus and the contents of RAM (DP_7, “1”, DP_5, DP_4, DP_3, DP_2, DP_1, and DP_0) specified by DP_6 = (“1”) are set to the L and K registers, respectively.

Remark Following combination are prohibited in OP or RT instruction

DST field = @KLR, SRC field = K or L register
DST field = @KLM, SRC field = K or L register
DST field and SRC field specify the same register
P-SELECT field = RAM, DST field = @MEM (for ALU operation)

JP INSTRUCTION

Mnemonic	BRCH field									Condition
	D_{21}	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	
JMP	1	0	0	0	0	0	0	0	0	Unconditional jump
CALL	1	0	1	0	0	0	0	0	0	Unconditional jump
JNCA	0	1	0	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	0	CA = 1
JNCB	0	1	0	0	0	0	1	0	0	CB = 0
JCB	0	1	0	0	0	0	1	1	0	CB = 1
JNZA	0	1	0	0	0	1	0	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	0	ZA = 1
JNZB	0	1	0	0	0	1	1	0	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	0	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	0	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	0	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	0	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	0	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	0	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	0	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	0	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	0	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	0	$DP_L = 0$
JDPLN0	0	1	0	1	1	0	0	0	1	$DP_L \neq 0$
JDPLF	0	1	0	1	1	0	0	1	0	DP_L = F (HEX)
JDPLNF	0	1	0	1	1	0	0	1	1	$DP_L \neq$ F (HEX)
JNSIAK	0	1	0	1	1	0	1	0	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	0	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	0	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	0	RQM = 1

JP INSTRUCTION

NA field											Jump address
D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	
0	0	0	0	0	0	0	0	0	0	0	Specify address 0 as jump address
0	0	0	0	0	0	0	0	0	0	1	Specify address 1 as jump address
0	0	0	0	0	0	0	0	0	1	0	Specify address 2 as jump address
to											to
1	1	1	1	1	1	1	1	1	1	1	Specify address 2047 as jump address

LD INSTRUCTION

ID field																HEX
D_{21}	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 0 0 1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0 0 0 2
to																to
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	F F F F

EFFECT OF ALU OPERATION ON FLAGS

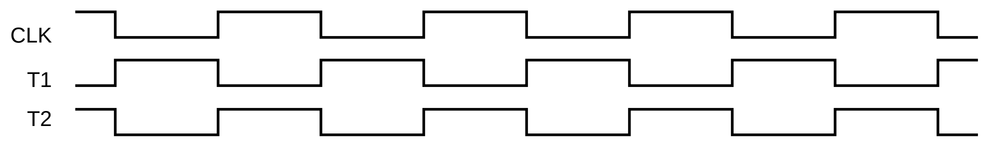
	Selected FLAG						Nonselected FLAG					
	S1	S0	C	Z	OV1	OV0	S1	S0	C	Z	OV1	OV0
NOP	●	●	●	●	●	●	●	●	●	●	●	●
OR	X	↕	0	↕	0	0	●	●	●	●	●	●
AND	X	↕	0	↕	0	0	●	●	●	●	●	●
XOR	X	↕	0	↕	0	0	●	●	●	●	●	●
SUB	↕	↕	↕	↕	↕	↕	●	●	●	●	●	●
ADD	↕	↕	↕	↕	↕	↕	●	●	●	●	●	●
SBB	↕	↕	↕	↕	↕	↕	●	●	←	●	●	●
ADC	↕	↕	↕	↕	↕	↕	●	●	←	●	●	●
DEC	↕	↕	↕	↕	↕	↕	●	●	●	●	●	●
INC	↕	↕	↕	↕	↕	↕	●	●	●	●	●	●
CMP	X	↕	0	↕	0	0	●	●	●	●	●	●
SHR1	X	↕	↕	↕	0	0	●	●	●	●	●	●
SHL1	X	↕	↕	↕	0	0	●	●	←	●	●	●
SHL2	X	↕	0	↕	0	0	●	●	●	●	●	●
SHL4	X	↕	0	↕	0	0	●	●	●	●	●	●
XCHG	X	↕	0	↕	0	0	●	●	●	●	●	●

← : Affects the result of operation
↕ : Affected by the result of operation
0 : Cleared to 0
1 : Set to 1
● : Retains the previous state
X : Undefined

4. INSTRUCTION EXECUTION TIMING

The μPD77C25 operates according to the external square wave applied to the CLK pin. This square wave is internally divided into two to generate two phases of clocks as shown for internal operation.

Internal Clock Timing



The instruction is executed as follows.

(1) An instruction is executed with two T2's.

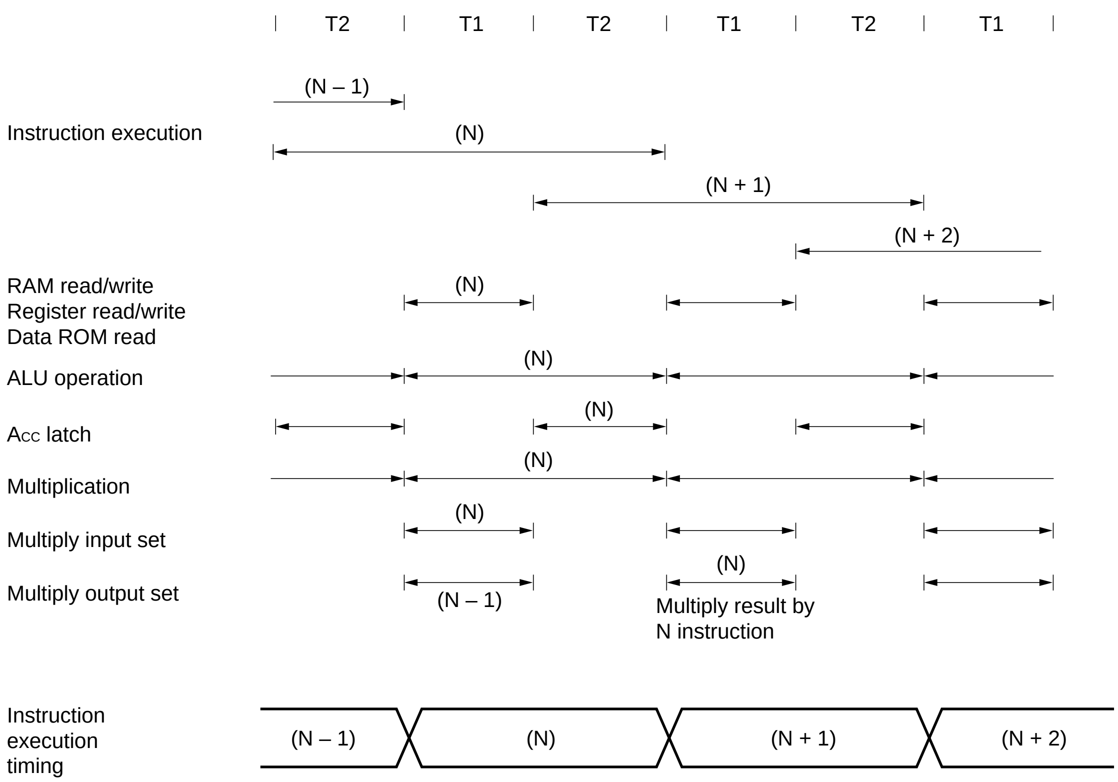
(2) Data is read from and written to RAM and registers and is read from the data ROM at T1.

(3) ALU performs an operation in T1 and T2 and the output result is latched to an Acc in one T2.

(4) The input data to the multiplier is set in one at T1. At the same time, a multiplication is performed and its result is output at the next T1.

The instruction execution timing in the timing chart indicates the cycle of T1 or T2.

Instruction Execution Timing



5. μPD77P25 PROM INTERFACE

(1) Input/Output Data Format

One word of the instruction ROM consists of 24 bits, while 16 bits make up one data ROM word. Data are programed to or read from these PROMs in units of 8 bits (byte). Therefore, special address are assigned to the PROMs. Address 0H through 1FFFH are assigned to the 2K-word instruction ROM. The following address, 2000H through 27FFH are assigned to the 1K-word data ROM.

Since the instruction ROM is configured on a 1-word-for-24-bit basis, one dummy byte address is provided per word. This dummy byte address is used for the instruction ROM code protection.

For example, data in word address 0H of the instruction ROM is equivalent to three bytes of byte address 0H to 2H. 3H is a dummy byte address.

Memory Map of μPD77P25 On-Chip PROM

(a) Instruction ROM (1 word = 24 bits)

24 bits | dummy byte

Internal Word Address	23 (MSB)	15	7	0 (dummy byte)
0H	0H	1H	2H	3H
1H	4H	5H	6H	7H
⋮	⋮	⋮	⋮	⋮
7FEH	1FF8H	1FF9H	1FFAH	1FFBH
7FFH	1FFCH	1FFDH	1FFEH	1FFFH

Remark Numeric values within the boxes are byte addresses of the instruction ROM.

(b) Data ROM (1 word = 16 bits)

16 bits

Internal Word Address	15 (MSB)	7 … 0 (LSB)
0H	2000H	2001H
1H	2002H	2003H
⋮	⋮	⋮
3FEH	27FCH	27FDH
3FFH	27FEH	27FFH

Remark Numeric values within the boxes are byte addresses of the data ROM.

(2) Erasing Data

The data in the μPD77P25D's UVEPROMs can be erased by exposing them to a light with a wavelength shorter than 400 nm. All data in the UVEPROMs are set to "1s" after the erasure.

Note that, if the μPD77P25D is exposed to the direct sunlight or fluorescent light for a long time, the data might be erased. To prevent this, the UVEPROM window must be masked with a cover or film for shielding from the ultraviolet light.

Usually, the UVEPROMs are erased exposed to the ultraviolet light with a wavelength of 254 nm. The total light quantity required to completely erase the written data is 15 Ws/cm^2 (UV intensity x erase time) that is equivalent to exposure to a UV lamp with a wavelength of 12000 $\mu W/cm^2$ for about 15 to 20 minutes. However, a longer erasing time may be required due to such factors as the life of the UV lamp and stains on the window of the package.

The μPD77P25D must be positioned within one inch away from the UV lamp.

(3) Procedure to Program Data

To Program data, perform the programming operation observing the following procedure.

<1> Apply +12.5 V to RST (pin 16), +6 V to V_{DD}, and +12.5 V to V_{PP}. This causes the PROMs to enter program mode.

<2> Specify the desired ROM byte address from address input pins A0 to A13.

<3> Program the data on the data bus (D0 to D7) by applying "0" to $\overline{CE}$ while $\overline{OE}$ is "1". (program mode).

<4> Output the programed data to the data bus (D0 to D7) by applying "0" to $\overline{OE}$ while $\overline{CE}$ is "1" (program verify mode).

<5> Repeat steps <2> through <4> 25 times maximum until the data is properly programed to the specified address.

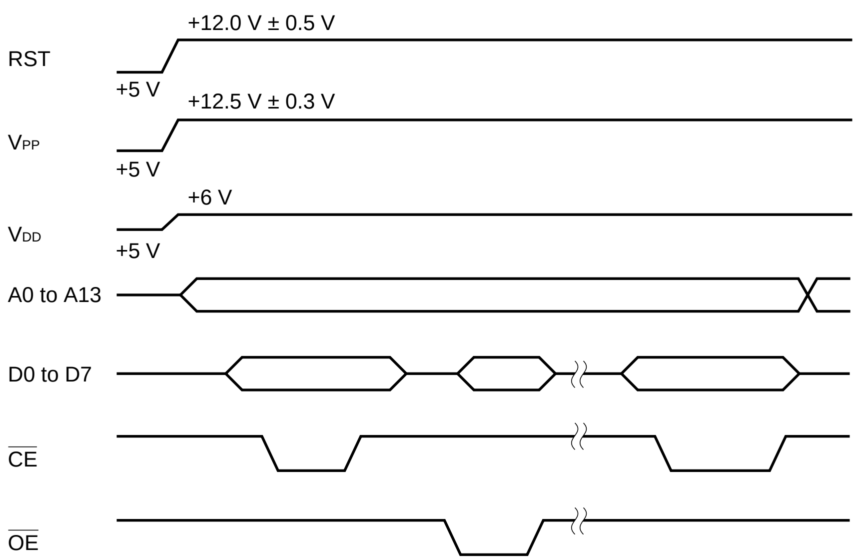
<6> After verifying that the data has been properly programed, apply additional pulses by setting $\overline{OE}$ to "1" (clear $\overline{CE}$ to "0". The pulse width of it is 3Xms if the number of repetitions in <3> and <4> is X).

The above procedure completes writing one byte of data.

In case the data will not be properly programed even after steps <2> to <4> have been repeated more than 25 times, it means that the μPD77P25 is defective.

Since the area from byte address 2800H to 3FFFH is for internal testing, the area to program data must be set from byte address 0H to 27FFH. Please set the data FFH to program data to the dummy byte address in the normal programming.

On-Chip PROM Program Timing



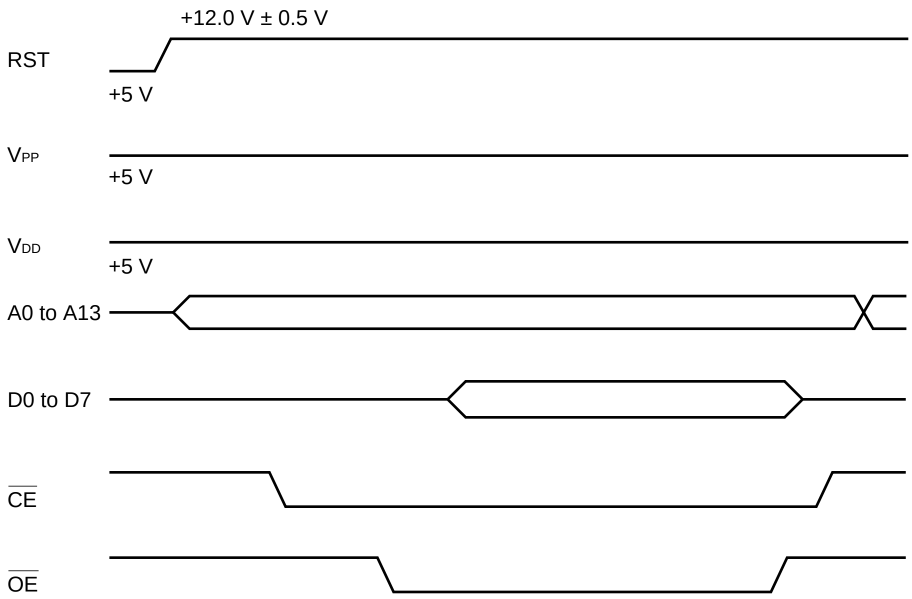
(4) Procedure to Read Data

<1> Apply +12.5 V to RST (pin 16), +6 V to V_{DD}, and +12.5 V to V_{PP}. This causes the PROMs to enter read mode.

<2> Specify the desired ROM byte address from the address input pins A0 to A13.

<3> Data will be output to the data bus (D0 to D7) by clearing $\overline{OE}$ and $\overline{CE}$ to "0".

On-Chip PROM Read Timing



(5) Instruction ROM code protection

A word of the instruction ROM can be protected if the data FEH is programmed to a dummy byte address. For example, the three bytes of addresses 0H through 2H (word address 0H) is protected if the data FEH is programmed to the dummy byte of address 3H. To protect the instruction ROM, perform the protecting operation observing the following procedure.

<1> Set the data FFH to the dummy addresses, then program the data as the procedure described (3).

<2> Verify the programmed data as the procedure described (4).

<3> Set the data FEH to the dummy addresses, then program the data as the procedure described (3).

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

<table>
<tr><th>Parameters</th><th>Symbol</th><th>Product names</th><th>Conditions</th><th>Ratings</th><th>Unit</th></tr>
<tr><td rowspan="3">Power Supply Voltage</td><td rowspan="2">V_{DD}</td><td>μPD77C25</td><td rowspan="2"></td><td rowspan="2">–0.5 to +7.0</td><td rowspan="6">V</td></tr>
<tr><td>μPD77P25</td></tr>
<tr><td>V_{PP}</td><td>μPD77P25</td><td></td><td>–0.5 to +13.5</td></tr>
<tr><td rowspan="3">Input Voltage</td><td rowspan="2">V_I</td><td>μPD77C25</td><td rowspan="2"></td><td rowspan="2">–0.5 to V_{DD} +0.5</td></tr>
<tr><td>μPD77P25</td></tr>
<tr><td>V_{RST}</td><td>μPD77P25</td><td>RST Pin</td><td>–0.5 to +13.0</td></tr>
<tr><td rowspan="2">Output Voltage</td><td rowspan="2">V_O</td><td>μPD77C25</td><td rowspan="2"></td><td rowspan="2">–0.5 to V_{DD} +0.5</td><td rowspan="2">V</td></tr>
<tr><td>μPD77P25</td></tr>
<tr><td rowspan="3">Operating Ambient Temperature</td><td rowspan="3">T_A</td><td>μPD77C25</td><td></td><td>–40 to +80</td><td rowspan="3">°C</td></tr>
<tr><td rowspan="2">μPD77P25</td><td>Normal operation</td><td>–10 to +70</td></tr>
<tr><td>PROM mode</td><td>+20 to +30</td></tr>
<tr><td rowspan="2">Storage Temperature</td><td rowspan="2">T_{stg}</td><td>μPD77C25</td><td rowspan="2"></td><td rowspan="2">–65 to +150</td><td rowspan="2">°C</td></tr>
<tr><td>μPD77P25</td></tr>
</table>

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Product names	Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	V_{DD}	μPD77C25	Normal operation	4.5	5.0	5.5	V
		μPD77P25					
		μPD77P25	Programming	5.75	6.0	6.25	
	V_{PP}	μPD77P25	Reading and normal operation	4.5	5.0	5.5	
			Programming	12.2	12.5	12.8	
Low Level Input Voltage	V_{IL}	μPD77C25		–0.3		+0.8	V
		μPD77P25					
High Level Input Voltage	V_{IH}	μPD77C25		2.2		V_{DD} +0.3	V
		μPD77P25					
Low Level Clock Input Voltage	V_{ILC}	μPD77C25		–0.3		+0.5	V
		μPD77P25					
High Level Clock Input Voltage	V_{IHC}	μPD77C25		3.5		V_{DD} +0.3	V
		μPD77P25					
Input Voltage for Setting PROM mode	V_{RST}	μPD77P25	Reading and writing	11.5	12.0	12.5	V
Operating Ambient Temperature	T_A	μPD77C25		–40	+25	+85	°C
		μPD77P25	Normal operation	–10		+70	
			PROM mode	+20		+30	

DC CHARACTERISTICS [NORMAL OPERATION] (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 4.5 V to 5.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level Output Voltage	V_{OL}	I_{OL} = 2.0 mA			0.45	V
High-level Output Voltage	V_{OH}	I_{OH} = –400 μA	0.7 V_{DD}			V
Low-level Input Leak Current	I_{LIL}	V_{IN} = 0 V			–10	μA
High-level Input Leak Current	I_{LIH}	V_{IN} = V_{DD}			10	μA
Low-level Output Leak Current	I_{LOL}	V_{OUT} = 0.47 V			–10	μA
High-level Output Leak Current	I_{LOH}	V_{OUT} = V_{DD}			10	μA
Supply Current (μPD77C25)	I_{DD}	f_{CLK} = 8.192 MHz		25	50	mA
		f_{CLK} = 8.192 MHz, RST = “1”		15	25	mA
Supply Current (μPD77P25)	I_{DD}	f_{CLK} = 8.192 MHz		35	60	mA
		f_{CLK} = 8.192 MHz, RST = “1”		20	35	mA
	I_{PP}				1	mA

DC CHARACTERISTICS [PROM MODE] (T_A = +20 to +30 °C, V_{DD} = 5.75 V to 6.25 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Leak Current	I_{RST}	V_{RST} = 12.0 ± 0.5 V			30	μA
Supply Current	I_{DD}				60	mA
	I_{PP}				30	mA

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK, SCK Input Capacitance	C_0	f_C = 1 MHz			20	pF
Input Capacitance	C_{IN}				20	pF
Output Capacitance	C_{OUT}				20	pF

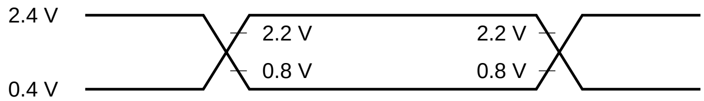
CLOCK TIMING REQUIREMENTS

Clock Timing (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ±10 %)

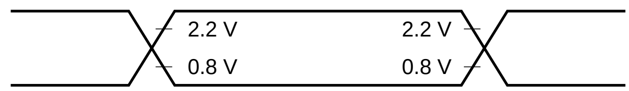
Parameters	Symbol	Product names	Conditions	MIN.	TYP.	MAX.	Unit
CLK Cycle Time	t_{CYC}	μPD77C25	Measuring at 2.0 V	120	122	2000	ns
		μPD77P25					
CLK Pulse Width	t_{CC}	μPD77C25	Measuring at 2.0 V	55			ns
		μPD77P25		60			
CLK Rise Time	t_{CR}	μPD77C25	Measuring at 1.0, 3.0 V			10	ns
		μPD77P25					
CLK Fall Time	t_{CF}	μPD77C25	Measuring at 1.0, 3.0 V			10	ns
		μPD77P25					
SCK Cycle Time	t_{CYS}	μPD77C25		240	244		ns
		μPD77P25					
SCK High Pulse Width	t_{SSH}	μPD77C25		100			ns
		μPD77P25					
SCK Low Pulse Width	t_{SSL}	μPD77C25		100			ns
		μPD77P25					
SCK Rise Time	t_{SR}	μPD77C25				20	ns
		μPD77P25					
SCK Fall Time	t_{SF}	μPD77C25				20	ns
		μPD77P25					

VOLTAGE REFERENCE LEVELS

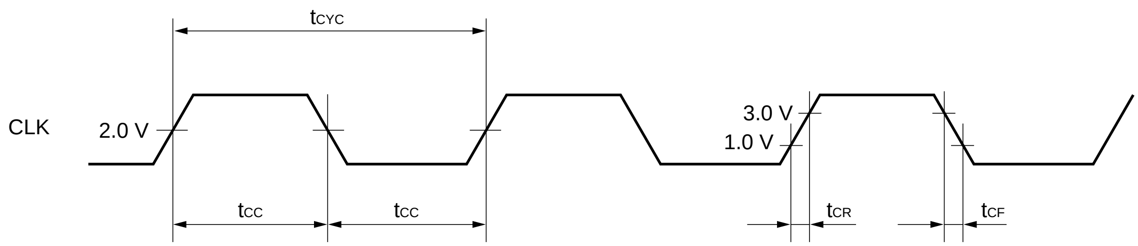
Input

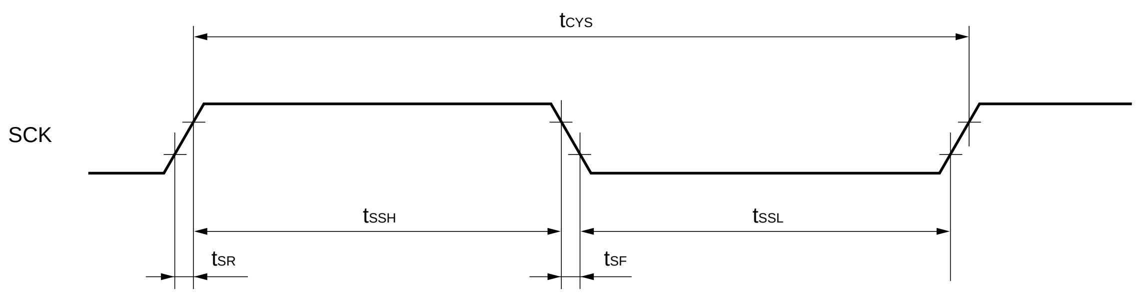


Output



TIMING CHART





HOST INTERFACE TIMING

Timing Requirement (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ±10 %)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
A0, $\overline{CS}$, $\overline{DACK}$ Setup Time for $\overline{RD}$	t_{SAR}		0			ns
A0, $\overline{CS}$, $\overline{DACK}$ Hold Time for $\overline{RD}$	t_{HRA}		0			ns
$\overline{RD}$ Pulse Width	t_{WRD}		120			ns
A0, $\overline{CS}$, $\overline{DACK}$ Setup Time for $\overline{WR}$	t_{SAW}		0			ns
A0, $\overline{CS}$, $\overline{DACK}$ Hold Time for $\overline{WR}$	t_{HWA}		0			ns
$\overline{WR}$ Pulse Width	t_{WWR}		120			ns
Data Setup Time for $\overline{WR}$	t_{SDW}		100			ns
Data Hold Time for $\overline{WR}$	t_{HWD}		0			ns
$\overline{RD}$, $\overline{WR}$ Recovery Time	t_{RV}		100			ns
$\overline{DACK}$ Hold Time for DRQ	t_{HRQA}		$0.5t_{CYC}$			ns
$\overline{RD}$, $\overline{WR}$ Setup Time for CLK	t_{SRWC}	**Note**	50			ns
$\overline{RD}$, $\overline{WR}$ Hold Time for CLK	t_{HCRW}	**Note**	50			ns

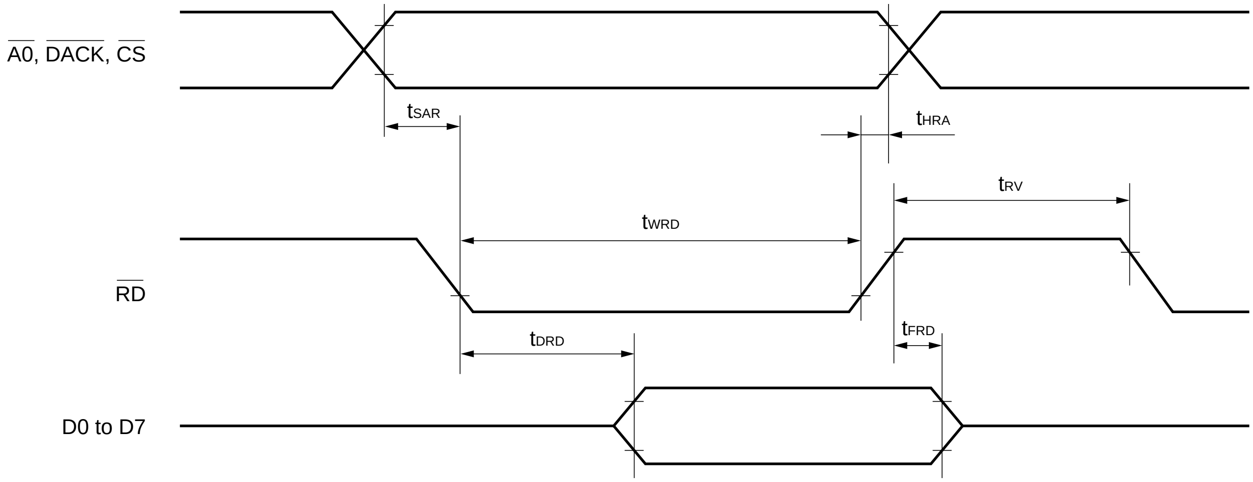
Note Setup and hold requirement for asynchronous signal only guarantee recognition at next CLK.

Switching Characteristics (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %, C_L = 100 pF)

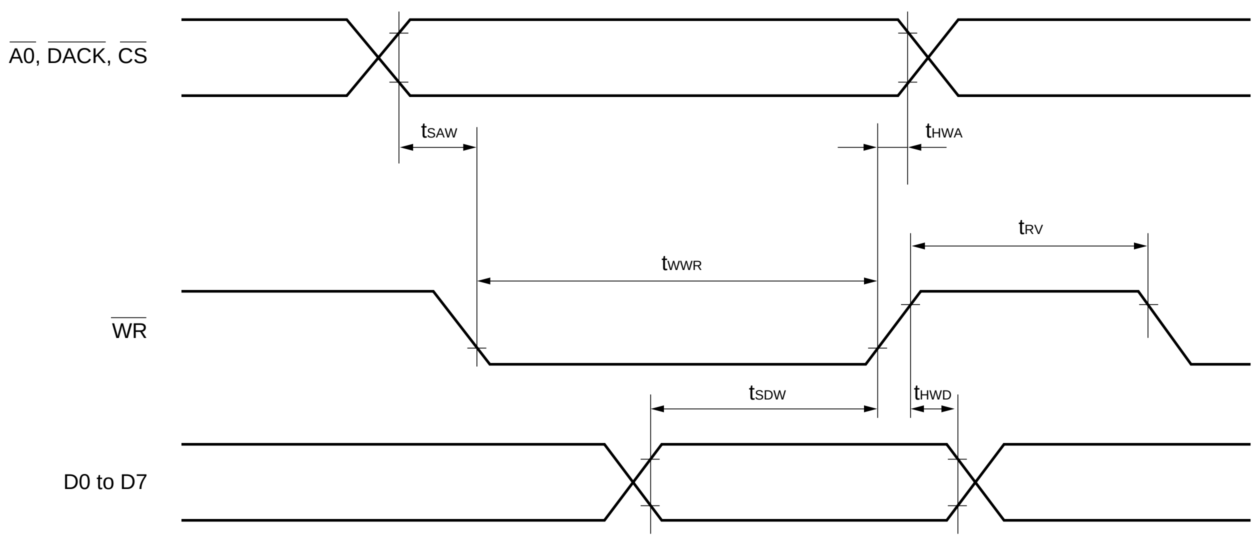
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{RD}$ ↓ → Data Delay Time	t_{DRD}				100	ns
$\overline{RD}$ ↑ → Data Float Time	t_{FRD}		10		65	ns
CLK ↑ → DRQ Delay Time	t_{DCRQ}				80	ns
$\overline{DACK}$ ↓ → DRQ Delay Time	t_{DARQ}				110	ns
CLK ↑ → P0, P1 Delay Time	t_{DCP}				100	ns

TIMING CHART

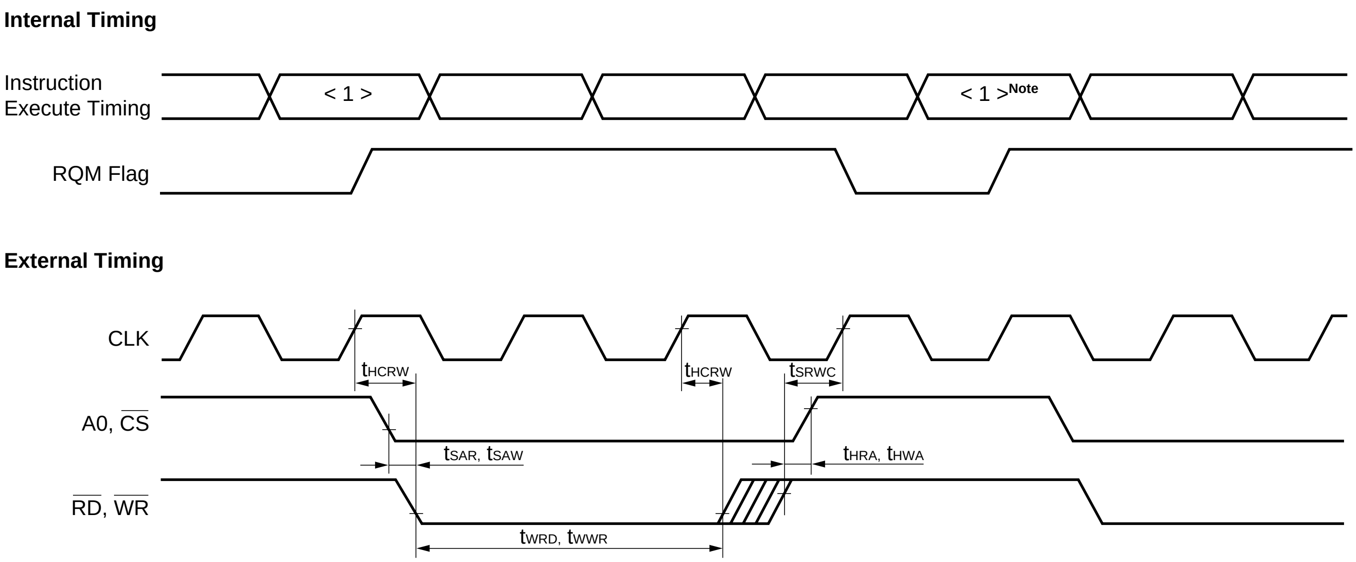
Host Read Operation



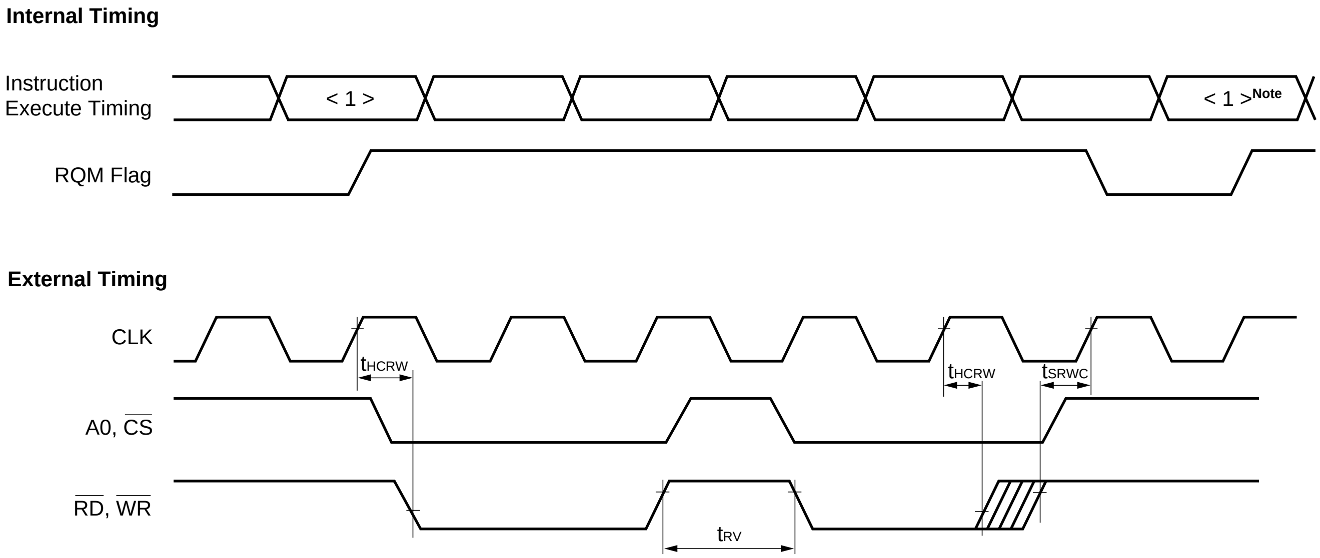
Host Write Operation



Normal Operation-1 8 bit Mode



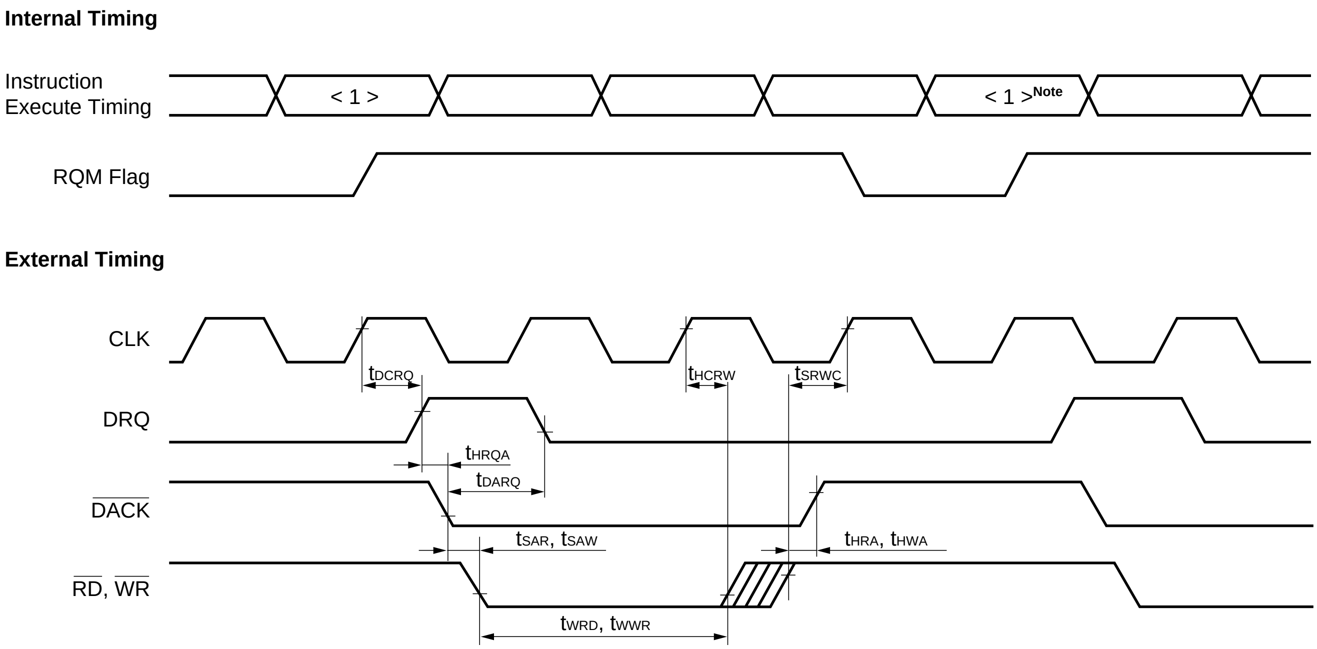
Normal Operation-2 16 bit Mode



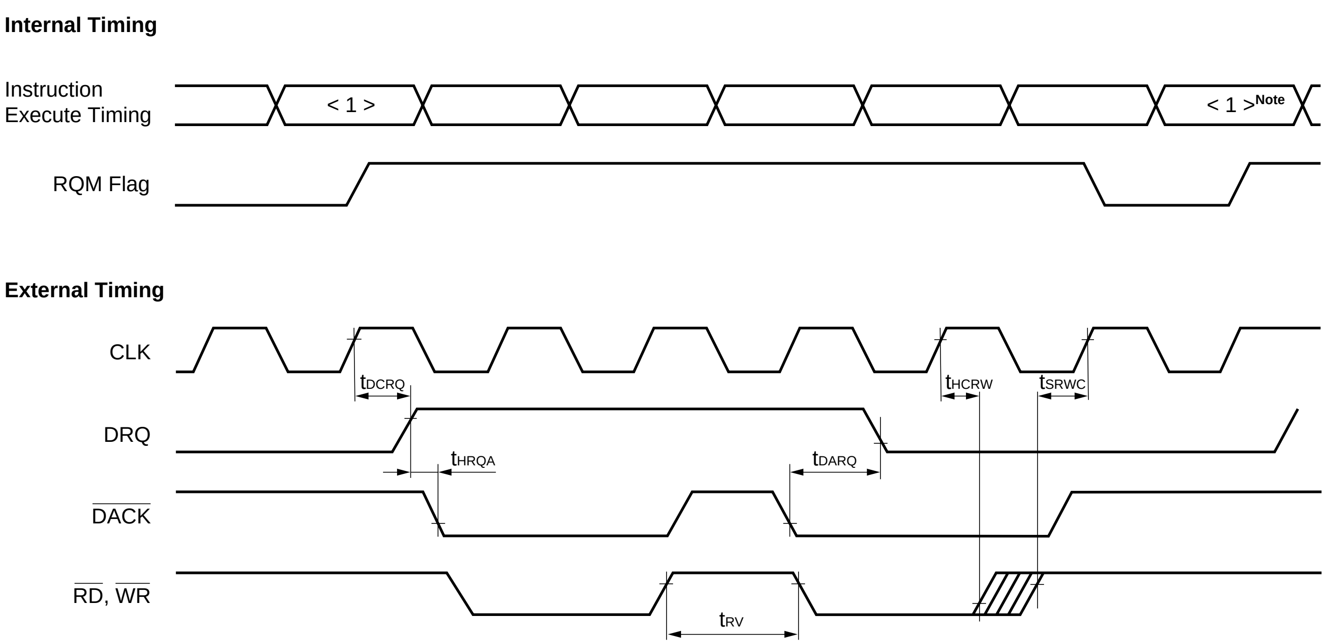
<1> Setting RQM flag to "1" (MOV @DR, xxx or MOV @xxx, DR)

Note The RQM flag is recognized as "0" from this instruction.

DMA Operation-1 8 bit Mode



DMA Operation-2 16 bit Mode

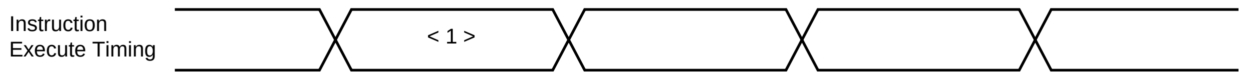


<1> Setting RQM flag to “1” (MOV @DR, xxx or MOV @xxx, DR)

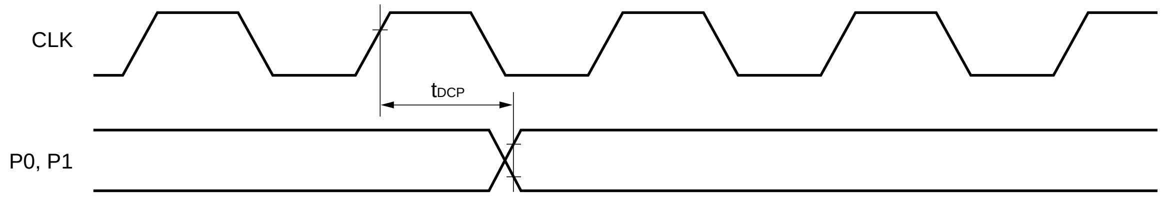
Note The RQM flag is recognized as “0” from this instruction.

Port

Internal Timing



External Timing



<1> Setting P0 or P1 (LDI @SR, I mm)

INTERRUPT RESET TIMING

Timing Requirements (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %)

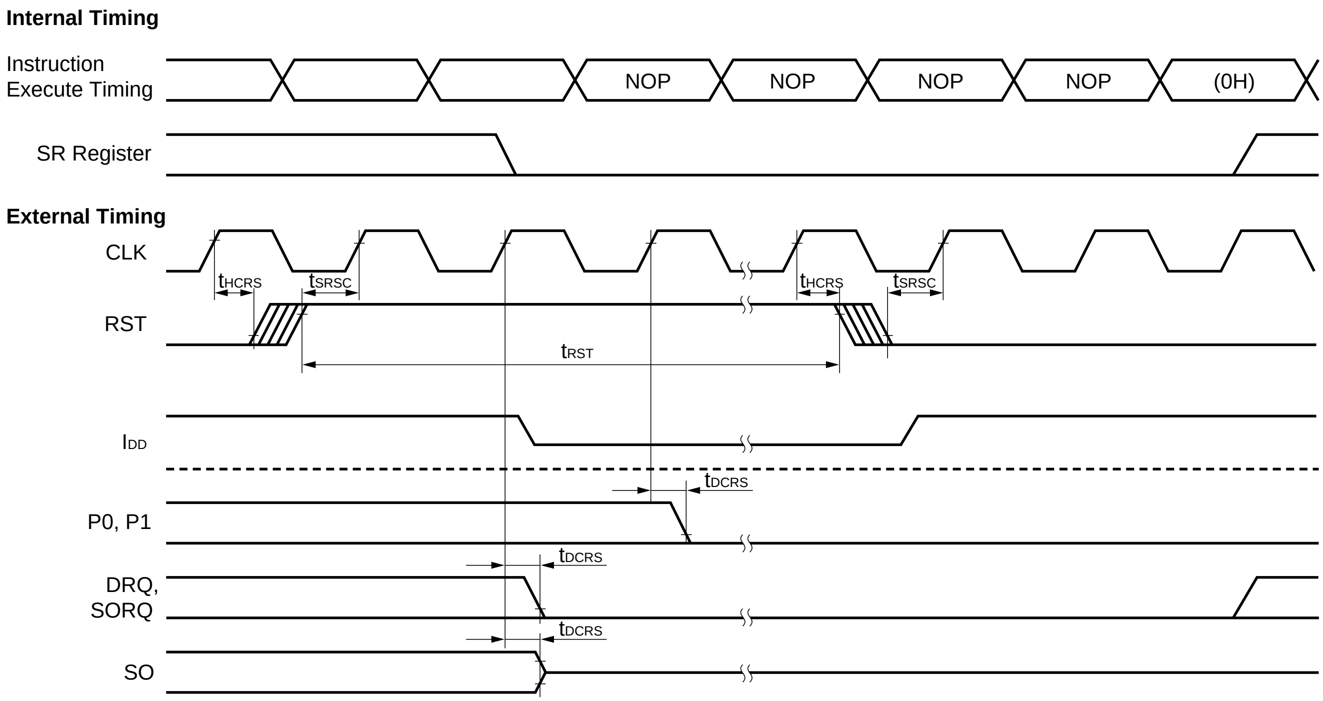
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RST Setup Time for CLK	t_{SRSC}	**Note**	50			ns
RST Hold Time for CLK	t_{HCRS}	**Note**	50			ns
RST Pulse Width	t_{RST}	System reset	$2t_{CYC}$			ns
		enter power saving state	$3t_{CYC}$			
INT Setup Time for CLK	t_{SINC}	**Note**	50			ns
INT Hold Time for CLK	t_{HCIN}	**Note**	50			ns
INT Pulse Width	t_{INT}		$3t_{CYC}$			ns
INT Recovery Time	t_{RINT}		$2t_{CYC}$			ns

Note Setup and hold requirement for asynchronous signal only guarantee recognition at next CLK.

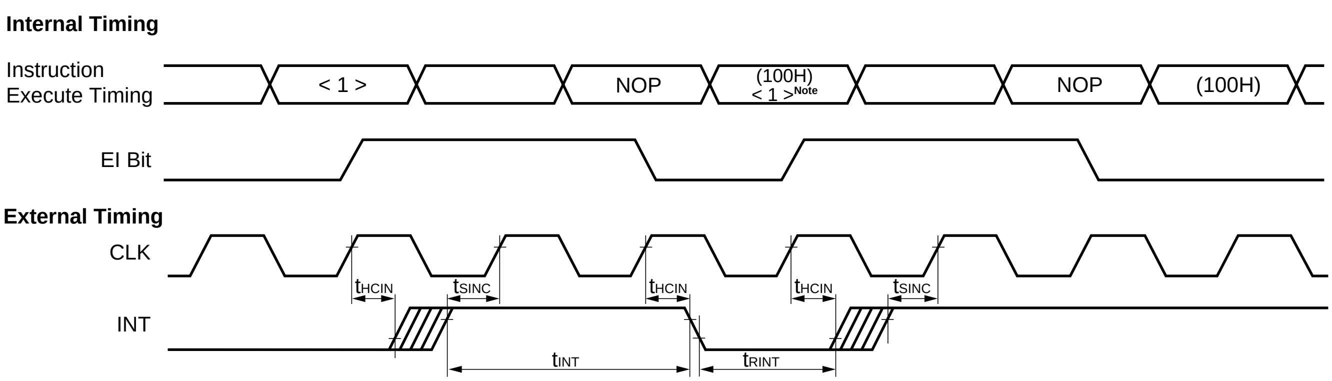
Switching Characteristics (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %, C_L = 100 pF)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK ↑ → Reset State Delay Time	t_{DCRS}				100	ns

Reset Operation



Interrupt Operation



<1> Setting EI bit to "1" (LDI @SR, I mm)

Note EI bit can be set to "1" from this instruction.

SERIAL INTERFACE TIMING

Timing Requirements (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SIEN}$, SI Setup Time for SCK	t_{SSIS}		50			ns
$\overline{SIEN}$, SI Hold Time for SCK	t_{HSSI}		30			ns
$\overline{SOEN}$ Setup Time for SCK	t_{SSES}		50			ns
$\overline{SOEN}$ Hold Time for SCK	t_{HSSE}		30			ns
CLK Setup Time for SCK	t_{SCS}	**Note**	50			ns
CLK Hold Time for SCK	t_{HSC}	**Note**	50			ns
SCK Setup Time for CLK	t_{SSC}	**Note**	50			ns
SCK Hold Time for CLK	t_{HCS}	**Note**	50			ns

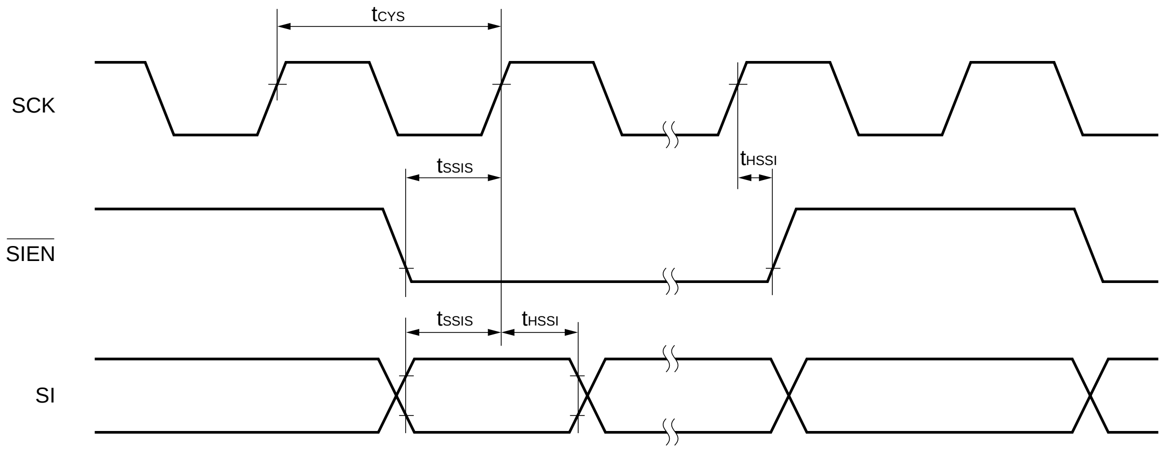
Note Setup and hold requirement for asynchronous signal only guarantee recognition at next CLK.

Switching Characteristics (μPD77C25: T_A = –40 to +85 °C, μPD77P25: T_A = –10 to +70 °C, V_{DD} = 5 V ± 10 %, C_L = 100 pF)

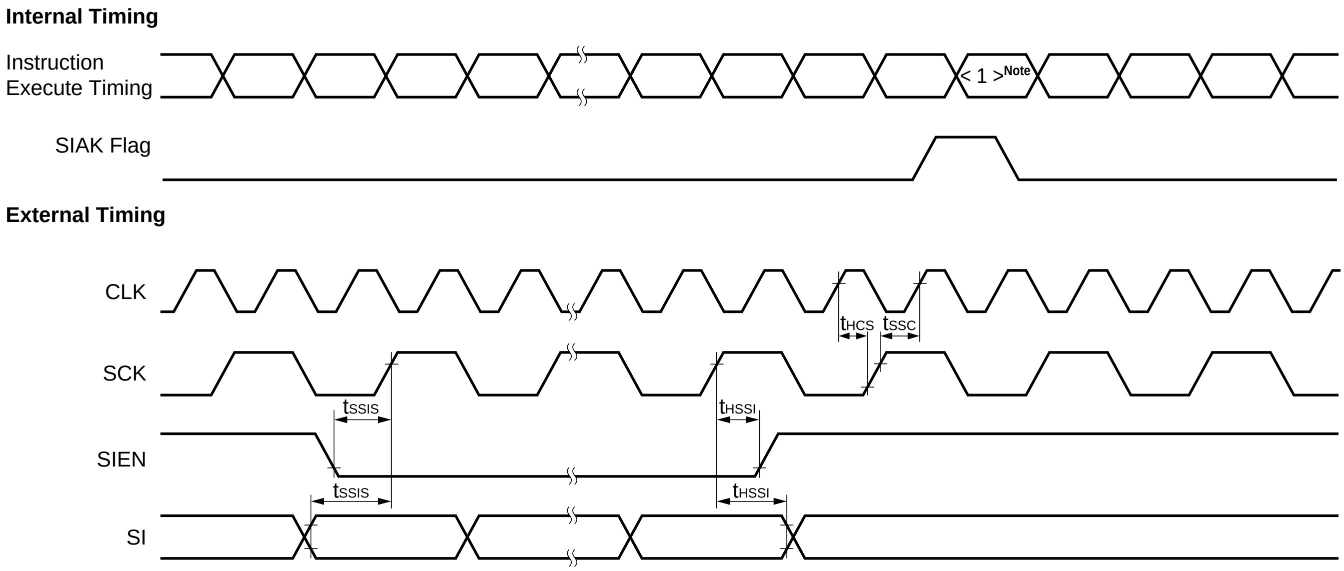
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK ↑ → SORQ Delay Time	t_{DSSQ}		30		150	ns
SCK ↓ → SO Delay Time	t_{DSLSO}				60	ns
SCK ↓ → SO Hold Time	t_{HSLSO}		0			ns
SCK ↓ → SO Float Time	t_{FSSO}				60	ns

TIMING CHART

Serial Input Operation



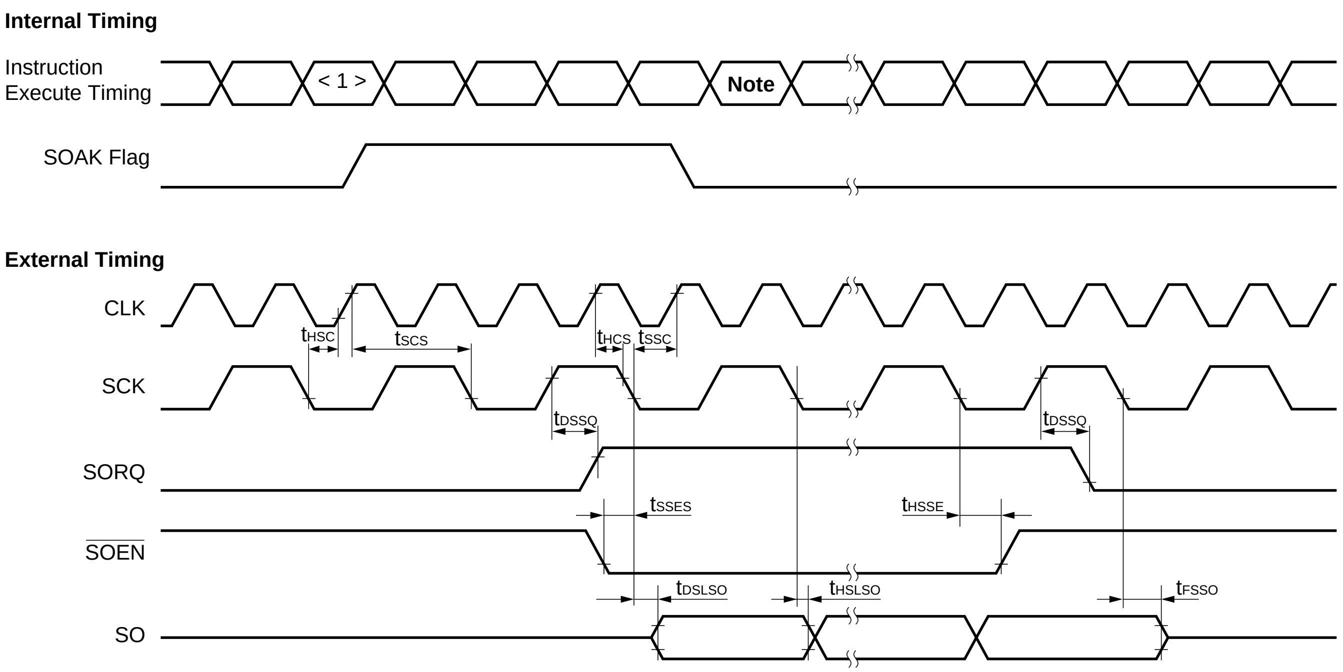
Serial Input Operation



<1> Setting SIAK flag to "0" (MOV @xxx, SI)

Note The SIAK flag is recognized as "1" from this instruction.

Serial Output Operation

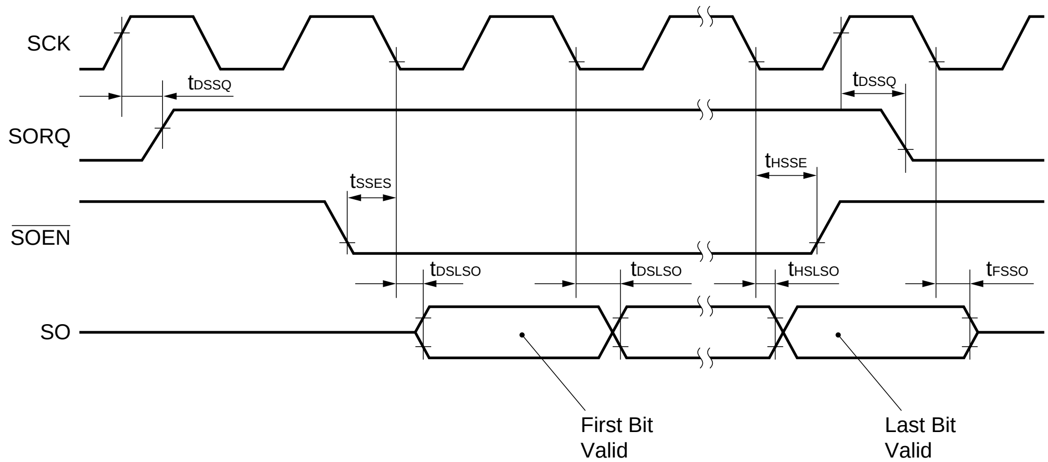


<1> Setting SOAK flag to "1" (MOV @SO, xxx)

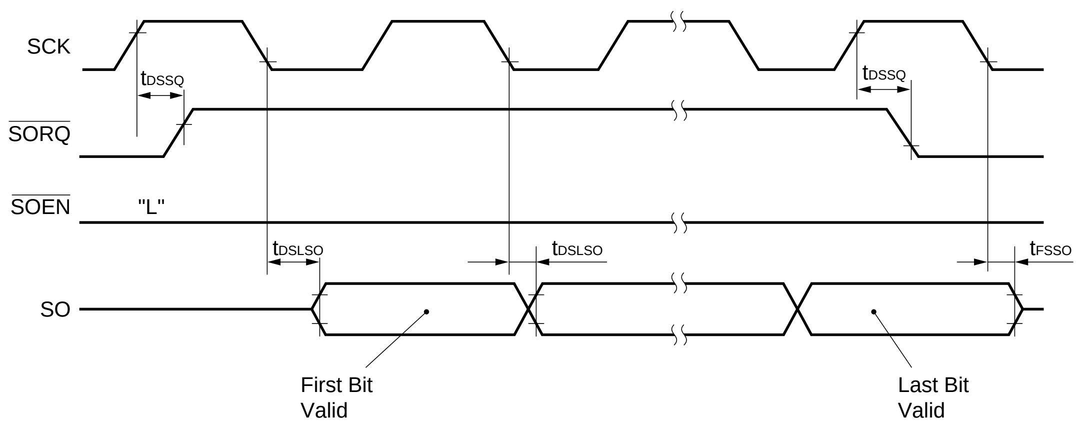
Note The SOAK flag is recognized as "0" from this instruction.

Serial Output Operation

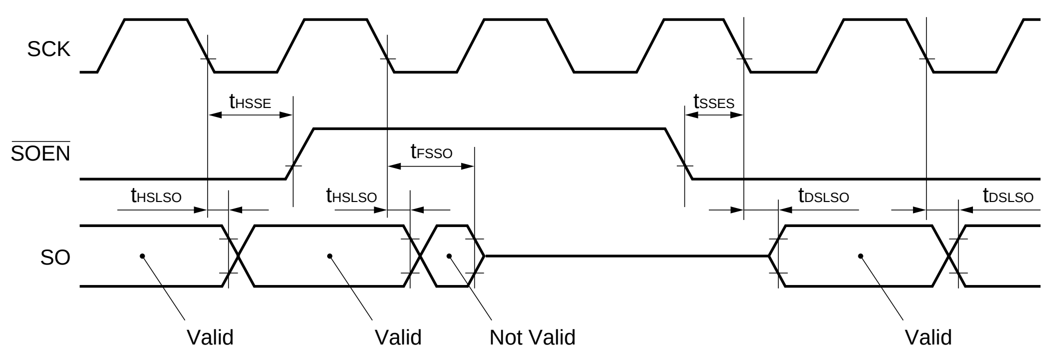
Serial Output Case #1: $\overline{\text{SOEN}}$ Asserted in Response to SORQ



Serial Output Case #2: $\overline{\text{SOEN}}$ Active before SORQ is High



Serial Output Case #3: if $\overline{\text{SOEN}}$ is Released in the Middle of a Transfer



UVPROM PROGRAMMING TIMING

DATA READ TIMING [PROM MODE]

Timing Requirements (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD}, V_{IHR} = 12.0 ± 0.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{CE}$ Setup Time for RST	t_{SRSCE}		2			μs
$\overline{OE}$ Setup Time for RST	t_{SRSOE}		2			μs

Switching Characteristics (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD}, V_{IHR} = 12.0 ± 0.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address to Output Delay	t_{DAD}				200	ns
$\overline{CE}$ to Output Delay	t_{DCD}				200	ns
$\overline{OE}$ to Output Delay	t_{DODR}				75	ns
$\overline{OE}$ High to Output Float	t_{FCD}		0		60	ns
Address to Output Hold	t_{HAD}		0			ns

DATA PROGRAM TIMING [PROM MODE]

Timing Requirements (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{IHR} = 12.0 ± 0.5 V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{CE}$ Setup Time for RST	t_{SRSCE}		2			μs
$\overline{CE}$ Setup Time for Address	t_{SAC}		2			μs
$\overline{CE}$ Setup Time for Data	t_{SDC}		2			μs
$\overline{CE}$ Setup Time for V_{PP}	t_{SVPC}		2			μs
$\overline{CE}$ Setup Time for V_{DD}	t_{SVDC}		2			μs
$\overline{OE}$ Setup Time for Data	t_{SDO}		2			μs
Address Hold Time	t_{HCA}		2			μs
Data Hold Time	t_{HCD}		2			μs
Initial Program Pulse Width	t_{WC0}		0.95	1.0	1.05	ms
Overprogram Pulse Width	t_{WC1} **Note**		2.85		78.75	ms

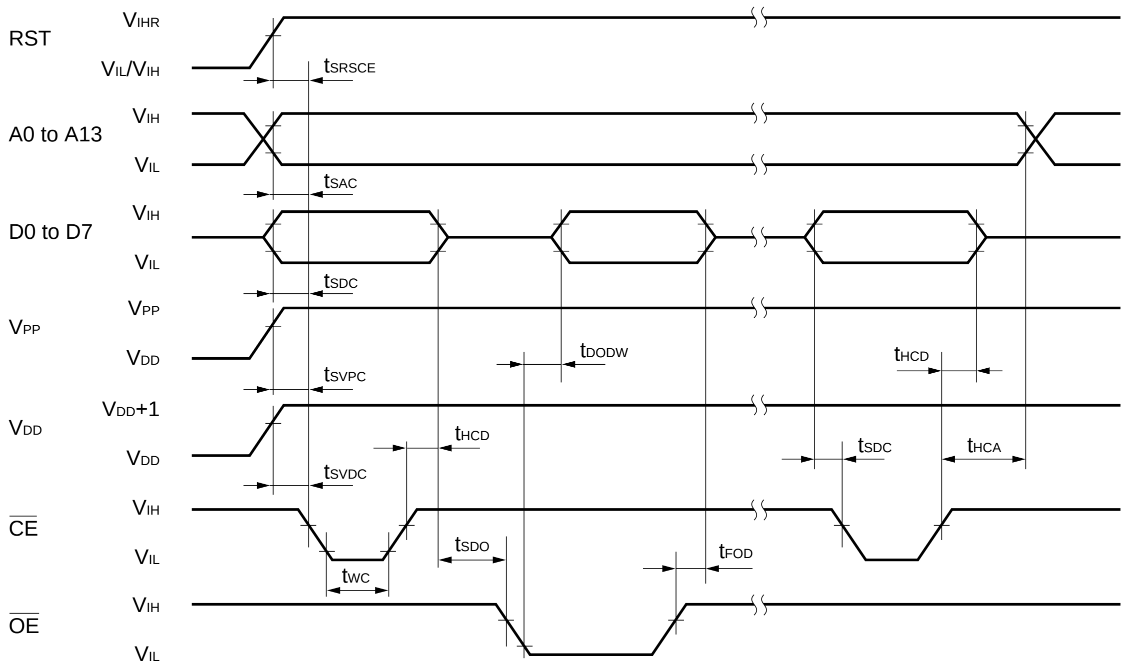
Note t_{WC1} = 3n t_{WC0} assuming initial program pulse is applied n times.

Switching Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{IHR} = 12.0 ± 0.5 V)

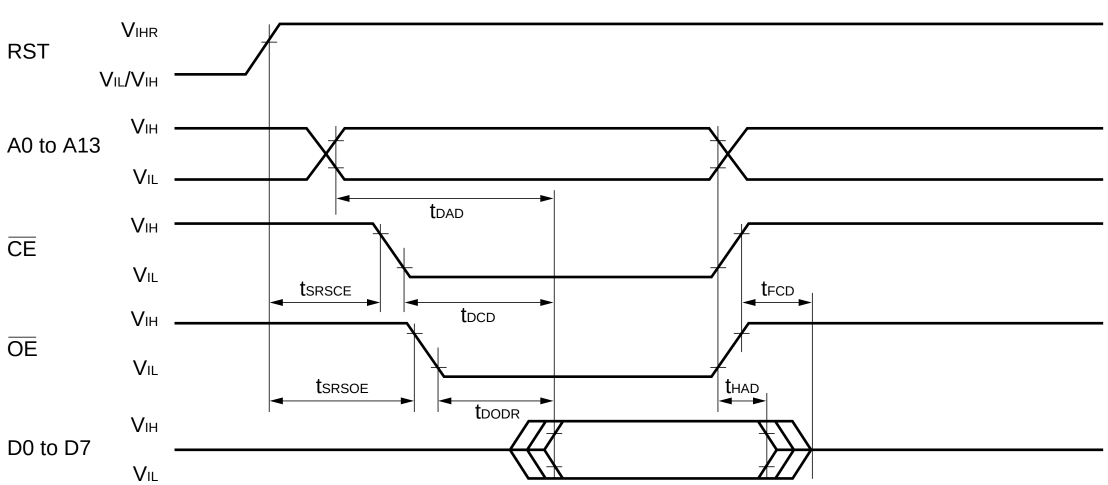
Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{OE}$ to Output Float Time	t_{FOD}		0		130	ns
$\overline{OE}$ to Output Delay	t_{DODW}				150	ns

TIMING CHART

PROM Program Operation

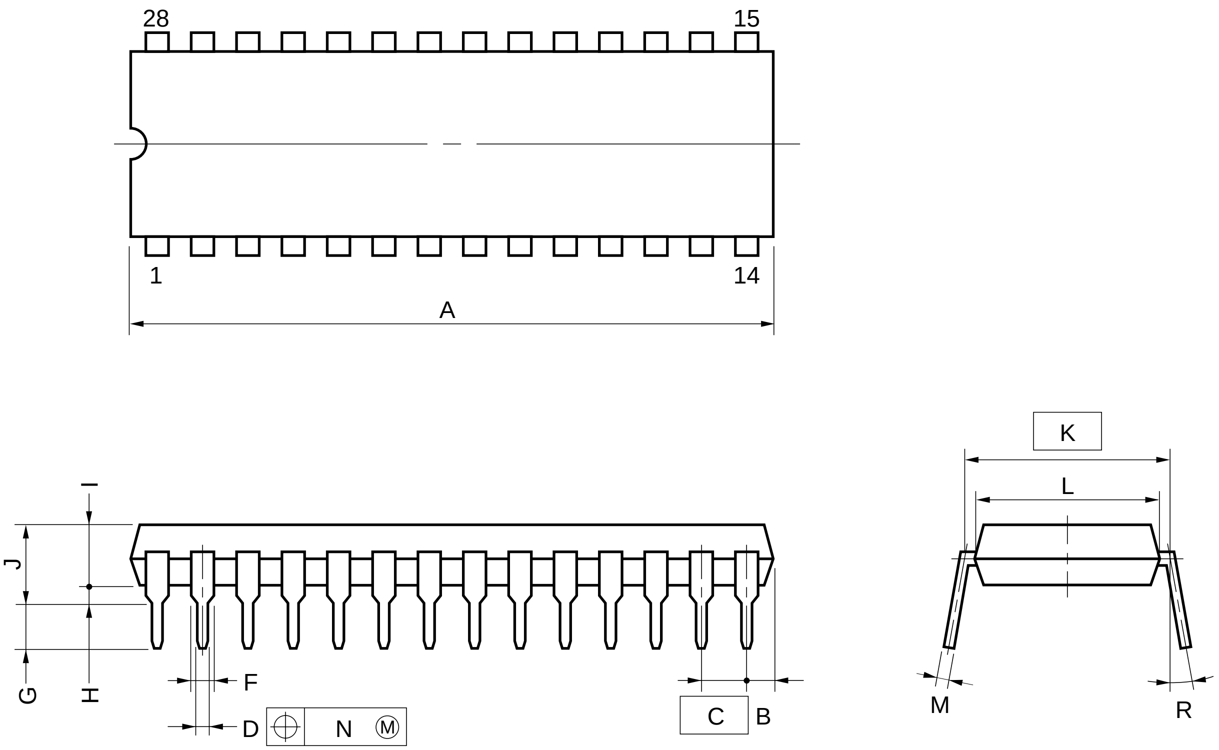


PROM Read Operation



7. PACKAGE DRAWINGS

28 PIN PLASTIC DIP (600 mil)



NOTES

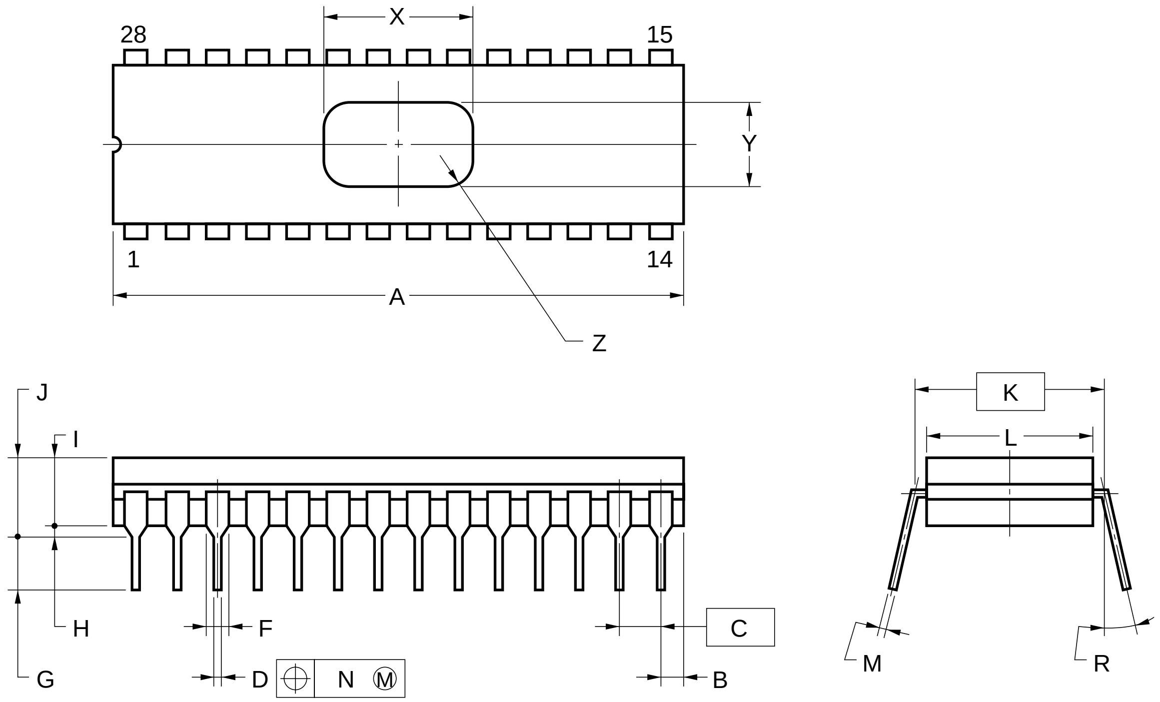
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	38.10 MAX.	1.500 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.6±0.3	0.142±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
R	0~15°	0~15°

P28C-100-600A1-1

28PIN CERAMIC DIP (600 mil)



NOTES

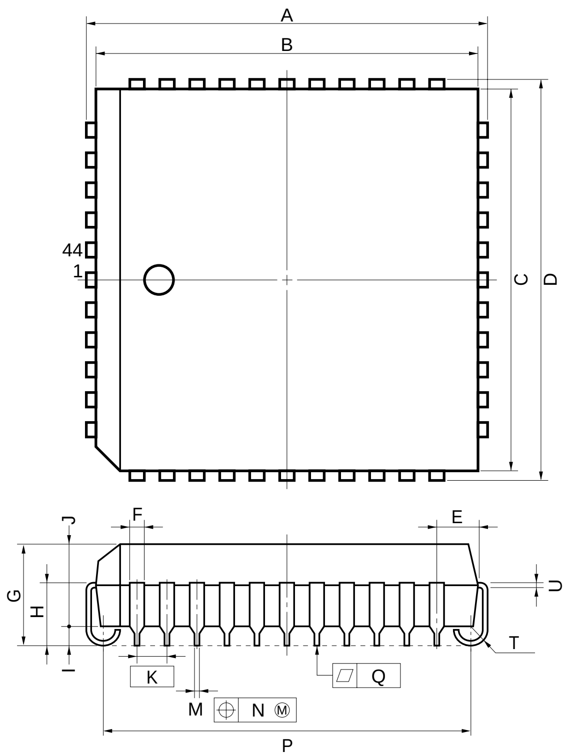
1) Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	38.10 MAX.	1.500 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.20 MIN.	0.047 MIN.
G	3.5±0.3	0.138±0.012
H	0.51 MIN.	0.020 MIN.
I	3.80	0.150
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	14.66	0.577
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.010
R	0~15°	0~15°
X	10.5	0.413
Y	9.2	0.362
Z	R2.0	R0.079

P28DW-100-600WA1-1

44 PIN PLASTIC QFJ (□650 mil)



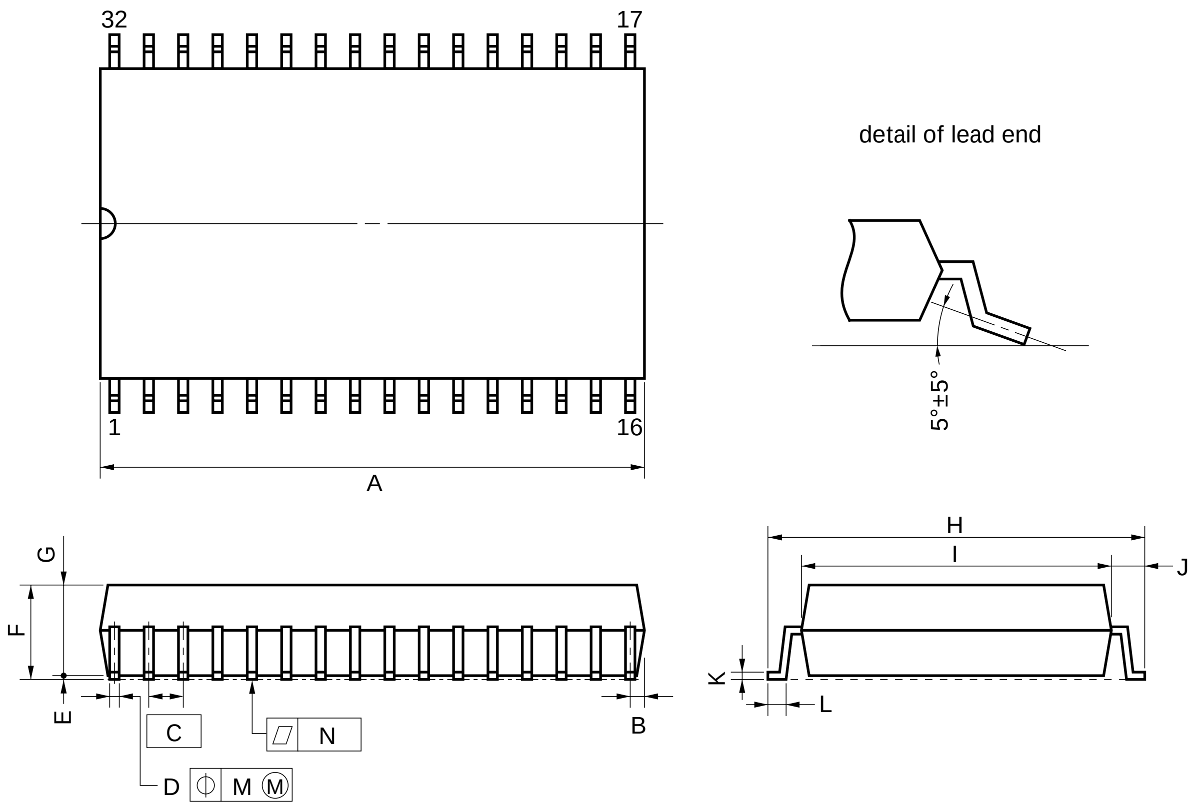
P44L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.5±0.2	0.689±0.008
B	16.58	0.653
C	16.58	0.653
D	17.5±0.2	0.689±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	15.50±0.20	$0.610^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

32 PIN PLASTIC SOP (525 mil)



S32GM-50-525A-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.61 MAX.	0.812 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.05±0.05	0.002±0.002
F	2.85 MAX.	0.113 MAX.
G	2.7	0.106
H	14.1±0.3	0.555±0.012
I	11.3	0.445
J	1.4	0.055
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

★ ## 8. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **“SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (C10535E)**.

Table 8-1 Surface mount devices

μPD77C25GW-xxx: 32-pin plastic SOP (525 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times, Exposure limit[Note]: 7 days (20 hours pre-baking is required at 125 °C afterwards).	IR35-207-2
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times, Exposure limit[Note]: 7 days (20 hours pre-baking is required at 125 °C afterwards).	VP15-207-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature), Exposure limit[Note]: 7 days (20 hours pre-baking is required at 125 °C afterwards).	WS60-207-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

μPD77P25GW: 32-pin plastic SOP (525 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 230 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 1 time, Exposure limit[Note]: 7 days (10 hours pre-baking is required at 125 °C afterwards).	IR30-107-1
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 1 time, Exposure limit[Note]: 7 days (10 hours pre-baking is required at 125 °C afterwards).	VP15-107-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Note Maximum allowable time from taking the soldering package out of dry pack to soldering.
Storage conditions: 25 °C and relative humidity of 65 % or less.

Caution Apply only one kind of soldering condition to a device, except for “partial heating method”, or the device will be damaged by heat stress.

μPD77C25L-xxx: 44-pin plastic QFJ (650 x 650 mil)

Process	Conditions	Symbol
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

μPD77P25L: 44-pin plastic QFJ (650 x 650 mil)

Process	Conditions	Symbol
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 1 time, Exposure limit[Note]: 2 days (16 hours pre-baking is required at 125 °C afterwards).	VP15-162-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

Note Maximum allowable time from taking the soldering package out of dry pack to soldering.
Storage conditions: 25 °C and relative humidity of 65 % or less.

Table 8-2 Through-hole devices

μPD77C25C-xxx: 28-pin plastic DIP (600 mil)
μPD77P25C: 28-pin plastic DIP (600 mil)
μPD77P25D: 28-pin ceramic DIP (600 mil)

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead).

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]